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A Novel Single-Phase Thirteen Level Inverter for Photovoltaic Application

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***Abstract*—This paper proposed a Single-Phase 13-level inverter with voltage control method using semiconductor power devices for photovoltaic systems . The multilevel voltage source inverters unique configuration allows them to make high voltages with low harmonics without use of transformers or series associated synchronized switching devices. The general role of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages for these reason multilevel inverters can simply provide the high power required of a large electric drives. The proposed inverter system gives superior voltage regulation, smooth results and efficiency compared to multi-level inverters. The inverter is capable of producing thirteen levels of output voltage levels (Vpv, 5Vpv/6, 4Vpv/6, 3Vpv/6, 2Vpv/6, Vpv/6, 0, -Vpv/6, -2Vpv/6, -3Vpv/6, -4Vpv/6, -5Vpv/6, -Vpv) .The proposed inverter was demonstrated by using simulation of MATLAB/SIMULINK software.**

Keywords; Photovoltaic system, H-Bridge inverter ,THD, multi-level inverter.

I. INTRODUCTION

The multilevel voltage source inverter is recently applied in many engineering applications such as ac power supplies, static VAR compensators, drive systems, etc. Multilevel inverters have been widely used in last year's for high-power applications **[1].** One of the major advantages of multilevel design is the harmonic diminution in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is collected of the number of levels of voltages, classically obtained from capacitor voltage sources. The so-called multilevel inverter starts from three levels. As the number of output levels reach infinity, the output total harmonics distortion (THD) approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping obligation, circuit design, and packaging constraints.

In the last time several topologies of multilevel inverters have been studied and presented. Among them, neutral point clamped inverters [2], and series connected cells inverters also called cascaded inverters [3]. The industry often has used the neutral-point-clamped inverter [4].flying capacitors inverters also called imbri-cated cells [5].

II. PHOTOVOLTAIC SYSTEMS

A photovoltaic system converts sunlight into electricity. A PV system contains different components including cells, electrical connections (series or parallels), mechanical mounting and a way to convert the electrical DC output. The electricity generated can be reserve in a standalone system, stored in batteries or can feed a bigger electricity power grid. It is motivating to include electrical conditioning apparatus. This one ensures the photovoltaic system to operate under optimum conditions. In this case, we use special equipment to track the maximum power of the array. This equipment is famous as maximum power point tracking(MPPT).

A simple model of a PV cell shows Figure 1. Rs is the series resistance associated with connecting to the active portion of a cell or module consisting of a series of equivalent cells. via Equation 1 and I-V measurements, the value of Rs can be calculated.

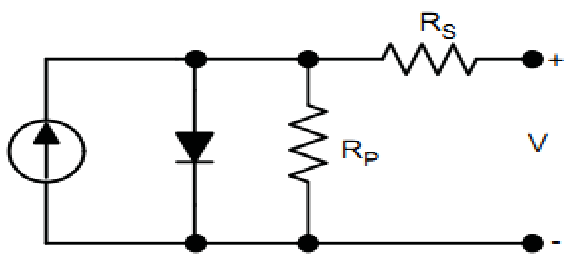

Figure 1. Equivalent Circuit of a PV model

Equation of PV output current:

$$I = I_{ph} - I_O \times (e^{\frac{q \times (V + I \times R_S)}{n \times k \times T}} - 1) - \frac{V + I \times R_S}{R_P}$$

Where:

- Io = Diode saturation current
- q = Electron charge (1.6x10-19 C)
- k = Boltzmann constant (1.38x10-23J/K)
- n = Ideality factor (from 1 to 2)
- T = Temperature (ºK)

The I-V characteristics of a realistic PV cell with maximum power point (MPP), short circuit current (Isc) and open circuit voltage (Voc) is shown in Figure 2. The MPP represents the point at which maximum power is obtained.
The parameters usually given in PV data sheets are:

- Voc = Open circuit output voltage
- Isc = Short circuit output current
- Vm= Maximum power output voltage
- Im = Maximum power output current

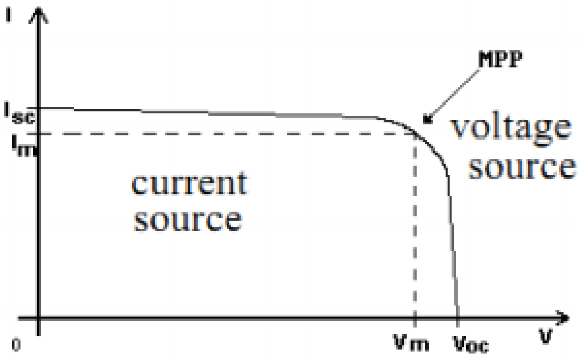

Fig.2 I-V Characteristic of the practical PV cell

III. PROPOSED METH

The all topologies presented in the multilevel inverter shows a number of characteristics in common. The main disadvantage associated with the multilevel inverter configuration is their circuit complexity, requiring a high number of power switches**[6].** When we are entering the simplified H-Bridge multilevel inverter, power devices will be diminution and circuit difficulty also reduction so circuit losses also reducing. Even taking into account the industrial tendency to lower the prize at which multilevel inverter can compete with standard configuration. This topology includes an H-Bridge stage with an supplementary bidirectional switch, drastically reducing the power circuit difficulty, and a modulator and firing control circuit developed using a controller.
The proposed H-bridge multilevel inverter achieves a diminution in the number of main switch required and uses no more diodes and capacitors that the second best topology, the asymmetric cascade configuration **[6]**.In the modulator circuit.

The single-phase simplified 13-level inverter proposed power circuit with supplementary switches is shown in figure.3.

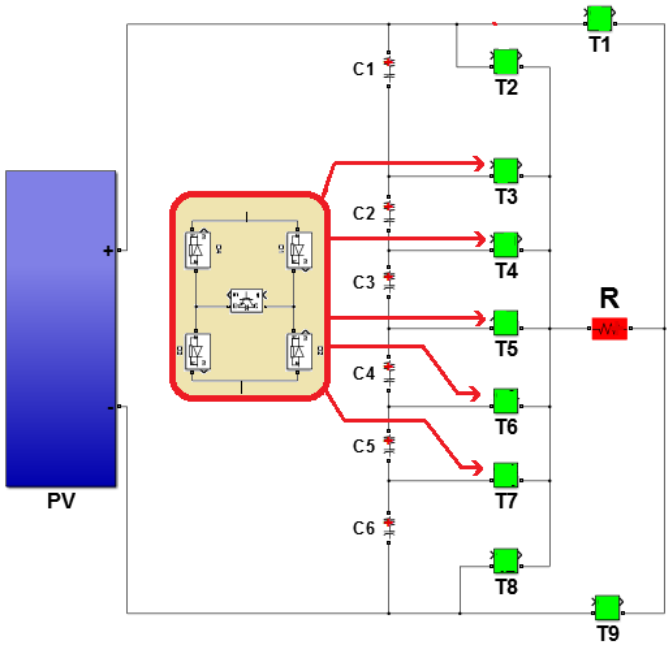

Fig.3. Simplified 13-level inverter proposed power circuit.

A. Hybrid H-Bridge Configuration

The block diagram of simplified H-bridge multilevel inverter that 13- level simplified H- bridge multilevel inverter **[6].** The H-bridge is created by four main power devices, S1 to S4. For 13 level output voltage, five auxiliary switches, four main switches and six capacitor requires.

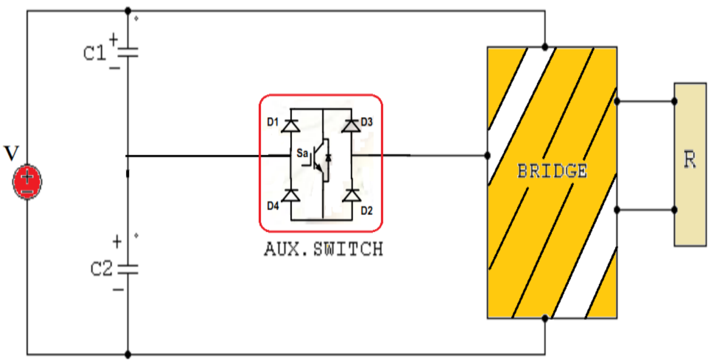

Fig.4. block diagram of simplified 13 level inverter.

In this context, we will provide an example of this technique. Fig. 5 shows the example Hybrid H-Bridge configuration. By using single Hybrid H-Bridge we can obtain 5 voltage levels. The number output voltage levels of cascaded Hybrid H-Bridge are given by 4n+1 and voltage step of each level is given by Vdc/2n [6]. Where n is number of H-bridges related in cascaded.

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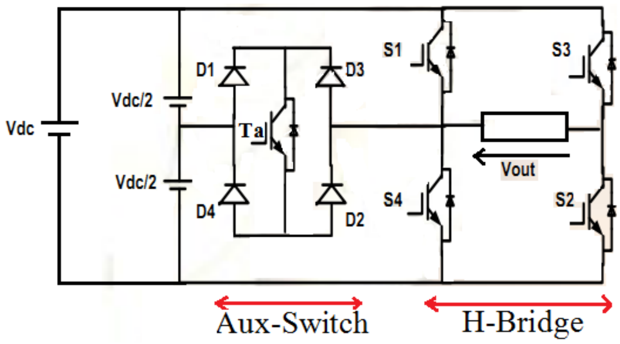

Figure. 5 Example Hybrid H-Bridges

The switching table of example Hybrid H-Bridge is given in Table 1.

Table 1. Switching table for example Hybrid H-Bridge

Output Voltage	Switches Turn ON
Vdc/2	Ta, S1
Vdc	S1,S2
0 Vdc	S4,D2
-Vdc/2	Ta,S3
-Vdc	S3,S4

B. Stage Advantages

1) lesser electromagnetic interference (EMI) and total harmonic distortion (THD).
2)They are appropriate for high voltage and high current applications.
3) Less difficulty of the circuit as the levels increase.
4) It consists of single-phase conventional H-bridge inverter, bidirectional secondary switches a capacitor voltage divider formed by capacitors.
5) enhanced output waveforms.
6) lesser filter size.
7) abridged number of switches employed.
8) The novel topology achieves a around 40% reduction in the number of main switches necessary, using only nine controlled power switches instead of twelve required in any of the other three configurations. The supplementary switch voltage and current rating are lesser than the once required by the main controlled switches.
9). No charge unbalance difficulty exists when the converters are in either rectification mode or in inversion mode.
10). They have very high efficiency because the switches are switching at a low frequency.

IV. MODE OF OPERATION

The operating principle of this inverter can be divided into thirteen, which has positive mode of operation and negative mode of operation.
The single-phase proposed is capable of producing thirteen different levels of output-voltage levels (*Vpv,5Vpv/6, 4Vpv/6, 3Vpv/6, 2Vpv/6,Vpv/6, 0Vpv, -Vpv/6,-2Vpv/6, -3Vpv/6, -4Vpv/6, -5Vpv/6, -Vpv*) from the DC supply voltage Vpv, shown in figure.6.

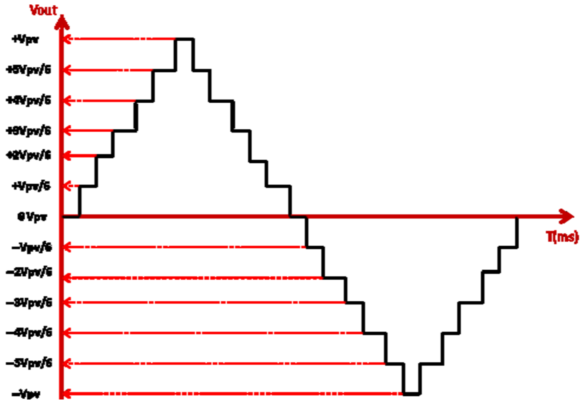

Fig. 6_ Single-phase proposed output voltage waveform

A. MODE 1(0 VOLTAGE LEVEL)

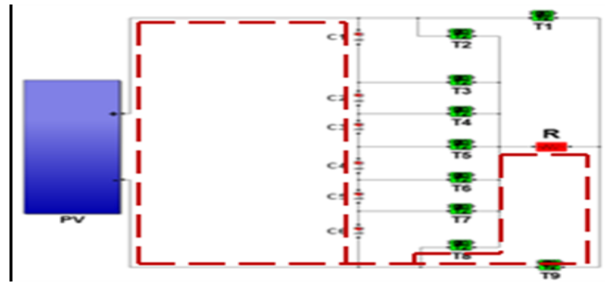

Fig.7.Mode of Operation 1(0Vpv)

The switch T8 is ON, connecting the load positive terminal to Vpv, and T9 is ON, connecting the load negative terminal to ground, Capacitors C1, C2, C3, C4, C5, C6 charging. lasting switches T1,T2, T3,T4, T5, T6, and T7 are OFF; the voltage across the load terminals R is 0Vpv.

B. MODE 2(VOLTAGE LEVEL: +Vpv/6)

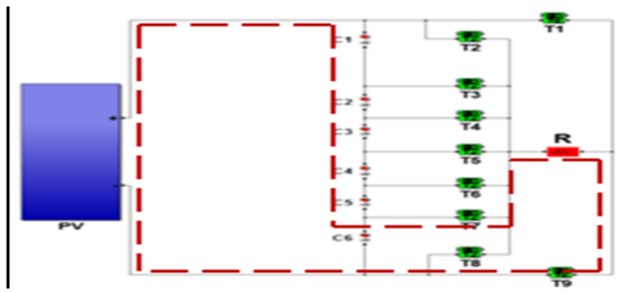

Fig.8.Mode of Operation 2(Vpv/6)

The switch T7 is ON, connecting the load positive terminal to Vpv, and T9 is ON, connecting the load negative terminal to ground, Capacitors C1, C2, C3, C4, C5 charging. lasting switches T1,T2, T3,T4, T5, T6, and T8 are OFF; the voltage across the load terminals R is Vpv/6.

C. MODE 3(VOLTAGE LEVEL: +2Vpv/6)

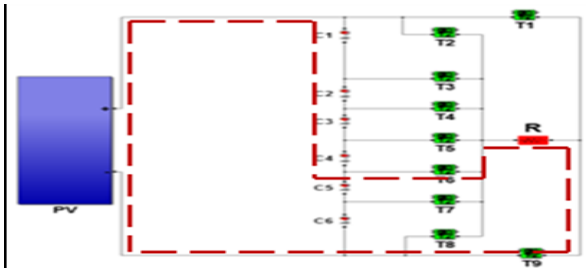

Fig.9.Mode of Operation 3(2Vpv/6)

The switch T6 is ON, connecting the load positive terminal to Vpv, and T9 is ON, connecting the load negative terminal to ground, Capacitors C1, C2, C3, C4 charging. lasting switches T1,T2, T3,T4, T5, T7, and T8 are OFF; the voltage across the load terminals R is 2Vpv/6.

D. MODE 4(VOLTAGE LEVEL: +3Vpv/6)

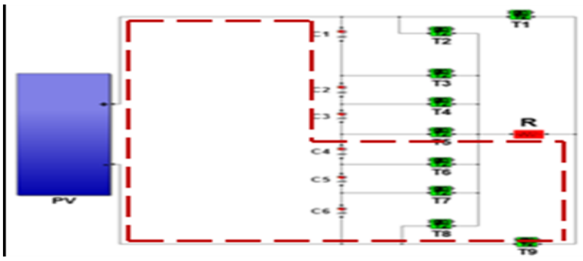

Fig.10.Mode of Operation 4(3Vpv/6)

The switch T5 is ON, connecting the load positive terminal to Vpv, and T9 is ON, connecting the load negative terminal to ground, Capacitors C1, C2, C3 charging. lasting switches T1,T2, T3,T4, T6, T7, and T8 are OFF; the voltage across the load terminals R is 3Vpv/6.

E. MODE 5(VOLTAGE LEVEL:+4Vpv/6)

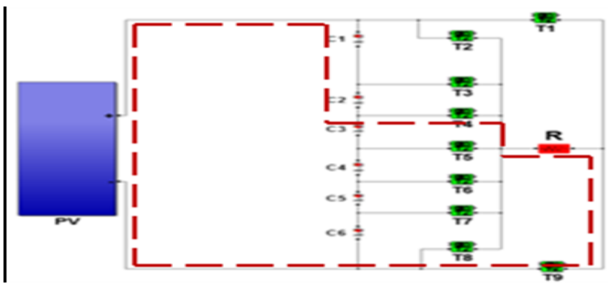

Fig.11.Mode of Operation 5(4Vpv/6)

The switch T4 is ON, connecting the load positive terminal to Vpv, and T9 is ON, connecting the load negative terminal to ground, Capacitors C1, C2 charging. lasting switches T1,T2, T3,T5, T6, T7, and T8 are OFF, the voltage across the load terminals R is 4Vpv/6.

G.MODE 6(VOLTAGE LEVEL:+5Vpv/6)

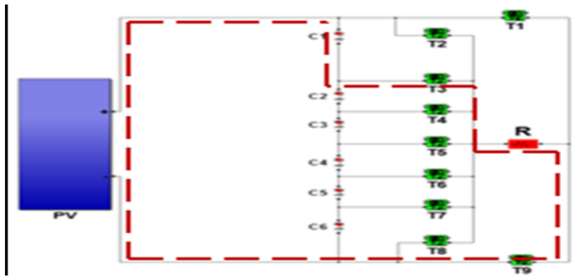

Fig.12.Mode of Operation 6(5Vpv/6)

The switch T3 is ON, connecting the load positive terminal to Vpv, and T9 is ON, connecting the load negative terminal to ground, Capacitors C1 charging. lasting switches T1,T2, T4, T5, T6,T7 and T8 are OFF; the voltage across the load terminals R is 5Vpv/6.

H. MODE 7(VOLTAGE LEVEL: +Vpv)

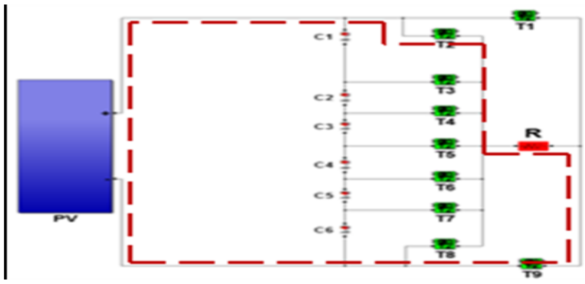

Fig.13.Mode of Operation 7(+Vpv)

The switch T2 is ON, connecting the load positive terminal to Vpv, and T9 is ON, connecting the load negative terminal to ground, lasting switches T1, T3,T4, T5, T6,T7 and T8 are OFF; the voltage across the load terminals R is Vpv.

I. MODE 8(VOLTAGE LEVEL:-Vpv/6)

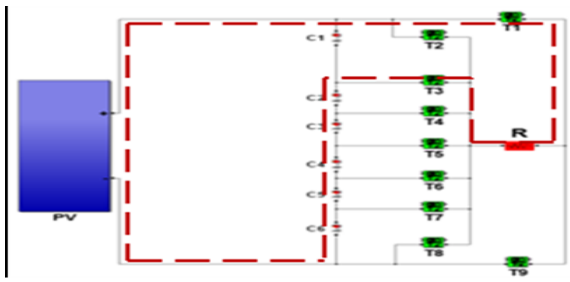

Fig.14.Mode of Operation 8(-Vpv/6)

The switch T1 is ON, connecting the load positive terminal to Vpv, and T3 is ON, connecting the load negative terminal to ground, Capacitors C2, C3, C4, C5, C6 charging. lasting switches T2,T4, T5, T6,T7,T8 and T9 are OFF; the voltage across the load terminals R is -Vpv/6.

J.MODE 9(VOLTAGE LEVEL: -2Vpv/6)

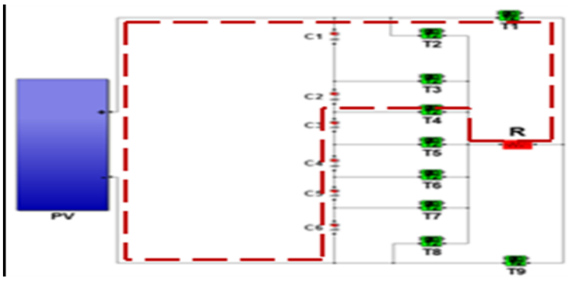

Fig.15.Mode of Operation 9(-2Vpv/6)

The switch T1 is ON, connecting the load positive terminal to Vpv, and T4 is ON, connecting the load negative terminal to ground, Capacitors C3, C4, C5, C6 charging. lasting switches T2,T3, T5, T6,T7,T8 and T9 are OFF; the voltage across the load terminals R is -2Vpv/6.

K.MODE 10(VOLTAGE LEVEL: -3Vpv/6)

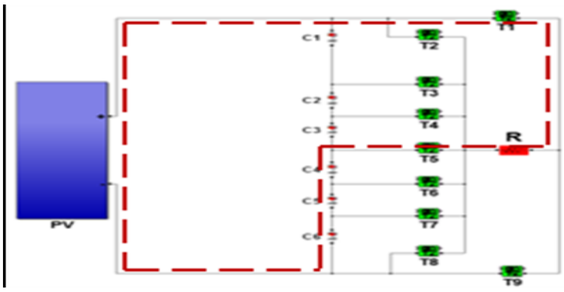

Fig.16.Mode of Operation 10(-3Vpv/6)

The switch T1 is ON, connecting the load positive terminal to Vpv, and T5 is ON, connecting the load negative terminal to ground, Capacitors C4, C5, C6 charging. lasting switches T2,T3, T4, T6,T7,T8 and T9 are OFF; the voltage across the load terminals R is -3Vpv/6.

L. MODE 11(VOLTAGE LEVEL: -4Vpv/6)

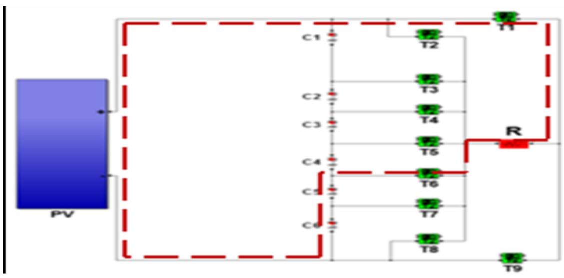

Fig.17.Mode of Operation 11(-4Vpv/6)

The switch T1 is ON, connecting the load positive terminal to Vpv, and T6 is ON, connecting the load negative terminal to ground, Capacitors C5, C6 charging. lasting switches T2, T3,T4, T5,T7,T8 and T9 are OFF; the voltage across the load terminals R is -4Vpv/6.

N. MODE 12(VOLTAGE LEVEL: -5VDC/6)

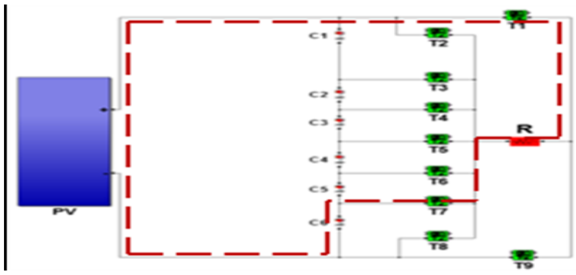

Fig.18.Mode of Operation 12(-5Vpv/6)

The switch T1 is ON, connecting the load positive terminal to Vpv, and T7 is ON, connecting the load negative terminal to ground, Capacitors C6 charging. lasting switches T2,T3,T4, T5, T6,T8 and T9 are OFF; the voltage across the load terminals R is -5Vpv/6.

O. MODE 13(VOLTAGE LEVEL: -Vpv)

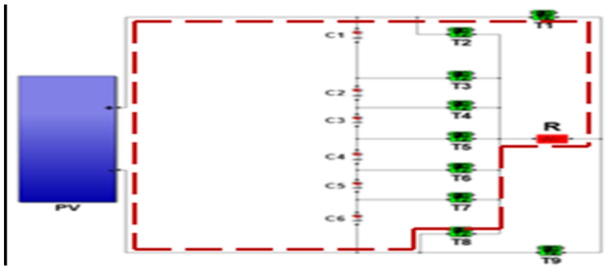

Fig.19.Mode of Operation 13(-Vpv)

The switch T1 is ON, connecting the load positive terminal to Vpv, and T8 is ON, connecting the load negative terminal to ground, lasting switches T2,T3,T4, T5, T6,T7 and T9 are OFF; the voltage across the load terminals R is -Vpv.

All possible cases (switch's and output voltage) are abbreviated in the table 2.

TABLET 2: SWITCHING COMBINATIONS REQUIRED TO GENERATE 13-LEVEL OUTPUT VOLT AGE WAVEFORM

Lavels	Vout	Switch's								
		T1	T2	T3	T4	T5	T6	T7	T8	T9
Lavel 01	Vpv	1	0	0	0	0	0	0	1	0
Lavel 02	5Vpv/6	1	0	0	0	0	0	1	0	0
Lavel 03	4Vpv/6	1	0	0	0	0	1	0	0	0
Lavel 04	3Vpv/6	1	0	0	0	1	0	0	0	0
Lavel 05	2Vpv/6	1	0	0	1	0	0	0	0	0
Lavel 06	Vpv/6	1	0	1	0	0	0	0	0	0
Lavel 07	0 Vpv	0	0	0	0	0	0	0	0	0
Lavel 08	-Vpv/6	0	0	0	0	0	0	1	0	1
Lavel 09	-2Vpv/6	0	0	0	0	0	1	0	0	1
Lavel 10	-3Vpv/6	0	0	0	0	1	0	0	0	1
Lavel 11	-4Vpv/6	0	0	0	1	0	0	0	0	1
Lavel 12	-5Vpv/6	0	0	1	0	0	0	0	0	1

Lavel 13	-Vpv	0	1	0	0	0	0	0	0	1

V . MATLAB/SIMULINK MODEL AND SIMULATION RESULTS

The Matlab Simulink model of the single-phase simplified Thirteen levels inverter and photovoltaic system circuit is shown in figure.20.
We used the following criteria in simulation;

a) Solar cell: open-circuit voltage (Voc) = 400 V
voltage at MPP (Vmpp) = 300 V
short-circuit current (Isc) = 14.25A
current at MPP (Impp) = 11.4 A

b) Inverter:
DC side capacitors Cl=C2=C3=C4=C5=C6=10000µF

c) Load :
current=3A, load power factor =1 .

This structure, developed using the Matlab/Simulink power system block set, comprises of components such as power electronic devices (MOSFETs) and elements such as capacitors and resistors.

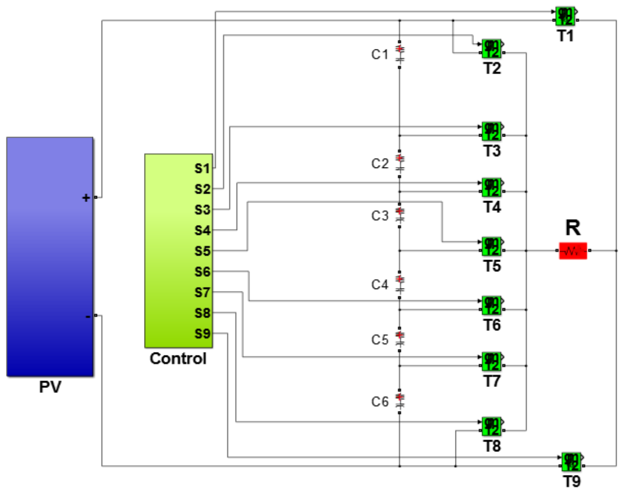

Fig. 20. Single-phase inverter and PV system simulation circuit

The all switching sequence generated by the block "Control" shown in fig 20, the figure 22 shows the simulated 13-level output voltage waveform of the proposed circuit.

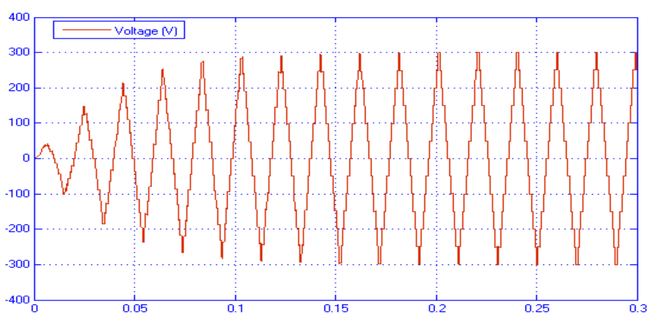

Fig. 22. Output voltage waveform of the simplified 13-level inverter proposed circuit.(Vpv bus =300V)

The Total Hannonic Distortion (THD) of the nine- level inverter is observed that 14.38 % and fundamental voltage is 240.4V(50Hz) that has been illustrated in figure. 23.

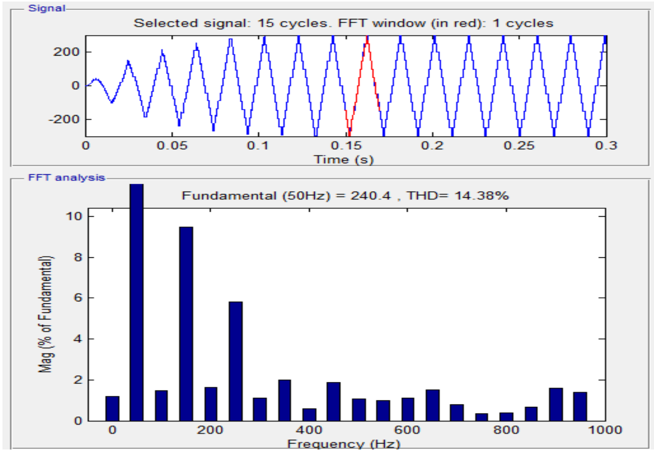

Fig. 23. THD of proposed system.

VI. CONCLUSIONS

This paper presented a new multilevel inverter with PV system sources, this inverter has been proposed for use in large electric drives. The performance of the proposed multilevel inverter was analyzed in detail. Simulation results have shown that with a control strategy operates the switches at the fundamental frequency, these converters have low output voltage THD and high efficacy and power factor, This shows the high efficiency of the proposed format.

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