

Processing and characterisation of silicon micro-rod solar cells

Thesis submitted in partial fulfilment of the
requirements of London South Bank University for
the degree of Doctor of Philosophy

By

Andrew Oates BEng

1st Supervisor: Prof H S Reehal

2nd Supervisor: Prof Y Bao

Feb 2017

Abstract

Silicon based solar cells are the dominant photovoltaic (PV) technology worldwide, but like any technology they must be subject to regular development to maintain this position. The refinement of raw silicon is an expensive process and significant cost reductions are achievable by reducing the bulk material usage. An indirect band-gap semiconductor, silicon is an inefficient absorber of light; therefore light trapping and absorption enhancing schemes are necessary to permit effective reduction in material usage. This is described as making the material optically thick but physically thin. A common approach to this problem is the fabrication of nano and micro-scale rod-like structures on the surface of thin silicon devices which decouple the optical absorption length from the electronic carrier collection distance. This has the added benefit of reducing the material quality requirement which is typically difficult to maintain for thin silicon as it would likely be deposited as a polycrystalline film rather than utilising conventional single crystal or multicrystalline wafers.

This project investigates the fabrication and performance of rod-like PV structures which have diameters on the low micron scale (1 μm and 10 μm). The design and fabrication of the structures is described together with results on their optical properties. These demonstrate an average reduction in reflection, compared to planar silicon, of 40% for the 1 μm diameter features and 10-20% for the 10 μm diameter features.

Various rod configurations were modelled optically by finite difference time domain (FDTD) simulations and comparisons of the modelled and measured reflection are presented. The results demonstrate good correlation and lend confidence to the use of modelling to inform the design of future structuring schemes. This was believed to be the first systematic study of identical geometry modelled and fabricated devices, particularly on the micron scale.

Proximity rapid thermal diffusion (PRTD) is developed as a doping technique and applied for emitter formation. It is believed that this is the first time that this process has been used in conjunction with structured devices for PV purposes. This approach permitted the formation of n-type emitters as shallow as ≈ 200 nm, with a diffusion time of less than three minutes and without the use of toxic process gases or diffusion specific hardware. Work undertaken to optimise the emitter formation process is described and results are presented which support the premise that whilst good absorption is clearly important in a solar cell, without an effective emitter, good efficiencies will remain out of reach.

Devices featuring 1 μm diameter rods confirmed this, proving challenging to form effective emitter layers on and were limited to matching planar device performance (conversion efficiency of 5.63% vs 5.64% for the planar control). Whilst subsequent refinement of the

emitter diffusion process demonstrated the potential to exceed planar performance, it reiterated the challenging nature of fabricating effective electronic devices involving features on this scale.

Conversely, devices with 10 µm diameter rods, whilst exhibiting more modest absorption improvements over equivalent planar devices, ultimately achieved peak efficiencies of 7.68%, a slightly greater than 2% absolute increase over their planar counterparts.

The open circuit voltage (V_{oc}) of all devices with length-diameter aspect ratios of 1:1 was found to be in the region 10-20 mV higher than that of a planar control device, whilst devices with 2:1 aspect ratio exhibited V_{oc} values which were broadly comparable to the control. This was generally contradictory to the literature which commonly reports V_{oc} reductions of 10-50 mV for devices with increased surface area compared to planar.

The development of various cell contacting schemes is discussed with a particular focus on aluminium doped zinc oxide (AZO), a transparent conductive oxide (TCO). In addition to the expected electronic properties, the sputter deposited films were found to possess useful anti-reflective performance. Results are presented for conformal coatings of AZO applied to rod structures, with 50-60% reduction in reflection demonstrated over planar silicon for 10 µm diameter rods and over 70% for 1 µm diameter features.

Acknowledgements

First and foremost I wish to thank my supervisor Professor Hari Reehal for his guidance throughout my project and thesis writing. Without his support and advice this PhD would have been a far more onerous and less rewarding experience.

In my day to day work I have had the privilege of sharing an office and laboratory with two colleagues and friends. Dr Jeremy Ball, with whom many tea fuelled discussions were shared and whose sense of humour has been invaluable in helping to maintain my sanity throughout this PhD. And Miss Cova Pardo Sanchez, who provided endless assistance with the recalcitrant ellipsometer and brought life and colour (pink!) to the office.

I would like to acknowledge Mr Jonathon Speed for his professional and expedient handling of matters of a technical and procurement nature, without whom, maintaining the smooth running of this project would have been a far more arduous task.

Thanks are owed to Dr Arti Agrawal and Mr Francisco Cabrera-España from City University for their collaboration in optically modelling the micro-rod devices that formed the basis of this work.

Thanks are also due to Philips Innovation Services, Eindhoven for providing fabrication capabilities and technical advice through the EUMINAfab framework.

The School of Engineering has provided support and equipment throughout this project and the EPSRC has provided ever important funding.

Finally, on a personal note, special thanks must go to my wonderful wife Katrina for her love, patience and good humour throughout this long process, without which none of this would have been possible. I also express my deepest gratitude to my parents for their endless support, both in my studies and in general. Not to mention for letting me take over their home office to complete my writing up.

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Nomenclature

μ c-Si:H	Microcrystalline hydrogenated silicon
AFM	Atomic force microscope
AM0	Air mass zero
AM1.5(G)	Air mass 1.5 (Global)
a-Si:H	Amorphous hydrogenated silicon
AR	Anti-reflective
AZO	Aluminium doped zinc oxide
BSF	Back surface field
BSR	Back surface reflector
c-Si	Crystalline silicon
CVD	Chemical vapour deposition
DRIE	Deep reactive ion etching
ECRCVD	Electron cyclotron resonance chemical vapour deposition
ERFC	Complementary error function
EQE	External quantum efficiency
FDTD	Finite difference time domain
FF	Fill factor
HIT	Heterostructure with intrinsic thin layer
HNA	An etch solution of hydrofluoric, nitric and acetic acids
IBC	Interdigitated back contact
ITO	Indium tin oxide
IQE	Internal quantum efficiency
I-V	Current-voltage
J_{sc}	Short circuit current density
LPCVD	Low pressure chemical vapour deposition
MESA	An edge isolation method (Not an acronym)
PC1D	Solar device modelling software
PECVD	Plasma enhanced chemical vapour deposition
PH_3	Phosphine
$POCl_3$	Phosphorous oxychloride
PRTD	Proximity rapid thermal diffusion
PTD	Proximity thermal diffusion
PV	Photovoltaic
RIE	Reactive ion etching

RTP	Rapid thermal processing
SEM	Scanning electron microscope
Si_3N_4	Silicon nitride
SiH_4	Silane
SiO_2	Silicon oxide
SOD	Spin on dopant
SRH	Shockley Read Hall
SSD	Solid state diffusion
TCO	Transparent conductive oxide
V_{oc}	Open circuit voltage

Chapter 1. Introduction

Despite a push for greater energy efficiency, the global demand for electricity continues to rise year on year [1]. There is much debate about the earth's remaining fossil fuel reserves and ever more creative means are found to access these stores. It is not in question, however, that such stores are in fact finite and a diversification of the planet's energy portfolio as a whole is crucial to prevent curtailment or loss of supply.

Renewable energy continues to climb the ladder in the global totals with a contribution of 4% in 2014 [2] but is still struggling to achieve mainstream penetration of the supply market. Despite this, whilst fossil fuels continue to dominate the market, a drive for the diversification of energy portfolios coupled with pollution reduction targets is helping to continue the upward trend in renewable uptake.

Solar energy in the form of photovoltaics (PV) is still a relatively small player in the renewable field but like renewable energy as a whole it is increasing its position at a substantial rate. Between 2015 and 2016, there was a 45% growth of the solar market and an associated fall in average price of 18% [3]. Whilst substantial, this rise is itself predicted to be eclipsed by a growth rate of 119% in 2016 with the US alone reaching its one millionth solar installation [4]. From a capacity point of view, the total global installed solar capacity exceeded 100 GW in 2012 which, although only a small fraction of total world demand, was 50 times more than ten years earlier [5]. By 2015 this total had more than doubled to nearly 230 GW, with 700 GW by 2020 believed to be achievable [6]. This remarkable growth rate, if sustained, would see solar become the dominant renewable technology over both wind and hydroelectric generation [7]. To see this goal achieved, however, demands that solar technology continue to increase in efficiency and decrease in cost.

The effect of increasing module efficiency on module cost can be illustrated by examining the influence of efficiency on levelised cost of energy (LCOE) of PV systems. The LCOE is generally defined as the average cost to build and operate a power generation system over its lifetime divided by the total energy output by the system over that lifetime [8]. Studies have shown that for a given module price in \$/W, more efficient PV modules result in lower LCOE systems [9]. Typically, a 1% absolute efficiency improvement can lead to a 4-5% decrease in the LCOE at the system scale.

What follows is a brief overview of PV technology with a view to placing this project in context.

1.1. First Generation Technology

Around 90% of global installed PV capacity is based on first generation crystalline silicon wafer technology which has seen significant development over its lifetime. This is despite the well understood limitations of silicon as a solar material and due in part to the sheer abundance of silicon's raw material, white quartzite sand.

The modern crystalline silicon solar cell originates from work done by Chapin, Fuller and Pearson of the Bell Telephone Laboratories in 1954 [10]. They observed a significant current flow when devices with a diffused P-N junction were exposed to light. Initial measures of performance yielded a conversion efficiency of 4.5% which was subsequently improved to 6% in short order [11].

The great driving force to improve efficiencies came about due to development for space applications. Improvements in absorption capabilities around the UV portion of the electromagnetic spectrum along with enhancements of antireflective front surface texturing by COMSAT Laboratories in 1971 took air mass zero (AM0) efficiencies to 13.5% [12]. AM0 refers to the radiation spectrum produced by the sun and unaffected by the earth's atmosphere which closely approximates a black body radiating at 5777K [13].

The addition of Back Surface Field (BSF) and Back Surface Reflector (BSR) technology to solar cells improved the red response and reduced absorption by the back contact further elevating performance to 16% [14].

Continual development has led to peak efficiencies in the region of 25% for crystalline silicon solar cells based on monocrystalline wafers [15]. This still falls short of the peak efficiency of $\approx 30\%$ for a 1.1 eV bandgap silicon cell as predicted by the Shockley–Queisser limit [16], indicating that there is still potential for enhancements to be made. A more detailed review of crystalline silicon technology is presented in Chapter 2.

1.2. Second Generation Technology

A significant proportion (as high as 50%) of the cost of crystalline silicon technology is the raw material, so in principle the simplest way to reduce cost is to reduce the amount of material used. This is commonly achieved by using thin layers of the semiconductor material and devices based on thin films are referred to as second generation solar cells. For crystalline silicon this approach is problematic as its indirect band gap [17] results in thin layers exhibiting poor absorption properties.

Hydrogenated amorphous silicon (a-Si:H) provides a partial solution to this problem, as the non-crystalline form of silicon is not bound by the rules of conservation of momentum and therefore acts like a direct band gap semiconductor [18]. Despite issues to do with material stability, development of a-Si:H has achieved peak efficiencies in the region of 14% as of 2016. However, since about 2006, the previously dominant (nearly 100%) thin film market share of a-Si:H has fallen to around 14% and been eclipsed by Cadmium Telluride (CdTe) [19].

CdTe is a direct band gap semiconductor with band gap energy of $\approx 1.5\text{eV}$. This combination makes it possible for a very thin ($<10\text{ }\mu\text{m}$) layer of CdTe to effectively absorb the vast majority of the visible solar spectrum. Extensive refinement of the technology and manufacturing process has resulted in the ability to fabricate complete modules at a dollar per watt (\$/W) cost equivalent to crystalline silicon ($\approx \$0.40/\text{W}$) [20] and with efficiencies of 18.6% [21]. Meanwhile, small area laboratory devices have reached efficiencies of 22.1% [21]. As a result, CdTe currently represents slightly greater than 57% of the thin film market and 4% of the global solar market share, arguably making it the only significant competitor to crystalline silicon. Despite these positives there are lingering concerns surrounding CdTe, mainly focused on the toxicity of cadmium and the questionable abundance of tellurium which possesses a rarity similar to platinum.

The current major competitor to CdTe is copper indium gallium selenide (CIGS) which as of 2015 possessed a 28% share of the thin film market. The technology has demonstrated a broadly comparable module efficiency of 17.5% [22] and small area laboratory device efficiency of 22.6% [21]. An advantage of CIGS is the lower toxicity of the constituent components compared to cadmium but the limited supply and price of gallium and indium are potential issues. The lower production rate of CIGS is predominantly due to the greater manufacturing complexity compared to CdTe which results in module production costs in the region of \$0.50/W [23]. However, recent estimates suggest that with adequate production scale, it should be possible to manufacture CIGS panels for \$0.40/W [24]. If achievable, this would place CIGS in direct competition with both CdTe and crystalline silicon from a cost point of view.

There is also significant interest in thin film PV devices which utilise earth abundant materials. The leading example of this approach is the use of kesterite compounds such as copper zinc tin sulphide (CZTS). Record device efficiency is still relatively low at 9.5% [25], however, the potential advantages of a cell that requires no rare or toxic materials are readily apparent.

1.3. Third Generation Technology

Third generation PV cells encompass a variety of technologies including dye sensitised, organic and polymer devices [26]. However, perhaps the most prevalent are those based on Perovskite compounds. These are typically a lead or tin halide-based material with an optical bandgap in the 1.5-2.3 eV range, encompassing the optimal value for a single junction cell. Arguably their greatest strength is the relative simplicity with which they may be manufactured. In principle, the cells may be prepared using only wet chemistry techniques, removing the need for costly vacuum deposition and high temperature processing typically required by first and second generation technologies. Also of note are the rapid efficiency improvements, rising from approximately 4% in 2009 [27] to 22% in 2016 [28]. The biggest challenge at present is maintaining the stability of the devices, as they degrade in standard environmental conditions with a particular sensitivity to moisture [29].

Another PV technology which falls under the third generation umbrella is the tandem cell concept. This approach circumvents the Shockley-Queisser limit by placing more than one junction in the optical path, each with a different band gap. Each junction effectively harnesses a different part of the solar spectrum and whilst a single junction cell is limited to a maximum of 33.16% (for a bandgap of 1.34 eV)[30], a triple junction cell could theoretically reach 63% [31]. The challenge for tandem devices is not only selecting materials with appropriate bandgaps but also materials which may be effectively stacked and interconnected in such a way that the electronic losses between the layers do not negate the gains of the tandem configuration.

A final technology to highlight, which also falls under the third generation umbrella, is that of nano and micro scale structuring of PV devices. This technology forms the basis of this body of research and is aimed predominantly at overcoming the material limitations preventing the development of efficient thin-film silicon solar cells.

1.4. Aims and Objectives

Despite being a first generation technology, crystalline silicon currently competes with the successful thin film technologies on module price and efficiency despite requiring a $\approx 200 \mu\text{m}$ wafer as opposed to a $\approx 1-2 \mu\text{m}$ absorber for CdTe and CIGS. Therefore, if a silicon cell could be fabricated which retained existing performance levels but with reduced material requirements it would gain a significant advantage over the competing technologies.

The challenge therefore is to overcome the problem of crystalline silicon's indirect band gap by fabricating a device that is physically thin but optically thick. Arrays of nanoscale

structures such as nanowires have seen significant investigation for this purpose and whilst they generally exhibit excellent absorption, their dimensions produce significant barriers to fabricating an effective electronic device due to issues such as increased carrier recombination losses.

This project attempts to resolve these device fabrication difficulties by increasing the structure size from the nano to the micro scale. Whilst this leads to an optical performance deficit, relaxation of the device fabrication tolerances results in cells whose improved electronic performance may effectively compensate for this. The structure geometry investigated is that of arrays of micro-rods (or micro-pillars) with diameters, lengths and inter-feature spacing on the low micron scale. Whilst the ultimate goal is the application of the features to thin silicon, as the purpose of this work is to assess the efficacy of the structures themselves, the formations are prepared on single crystal silicon wafers at this stage. Note that, in this work, the terms rod and pillar both appear and are used with equivalent meaning.

The overall aim of the project was to fabricate radial geometry solar cells based on crystalline silicon micro-rods and characterise and analyse their performance

The objectives were as follows:

- Establish the preferred geometry of structures and array configurations for investigation
- Establish a means by which to form a p-n junction on the structured arrays, i.e. grow or diffuse an emitter layer
- Establish the necessary ancillary techniques required to produce complete devices, i.e. contacts, anti-reflective coatings, passivation layers
- Measure and analyse the optical and electronic performance of the devices and compare to equivalent planar devices
- Develop an understanding of device operation, the factors controlling performance and routes to improved performance

1.5. Collaborations

Whilst there was significant literature on nano-scale structuring of silicon, there was less existing knowledge on larger, micron scale structures. This created a need for more information about preferred structure dimensions and arrangements and led to a collaborative modelling effort with City University London as a means to assess proposed pillar array designs. From this collaboration, finalised parameters for the pillar arrays to be

investigated were selected. This is described in Chapter 5. The collaboration with City was extended to include modelling of the optical behaviour of the silicon micro rod structures and comparison with the optical data measured at LSBU and this is also reported in Chapter 5.

Fabrication of the micro rod structures was initially planned to be carried out in-house. However, the available processing tools were not capable of providing suitably fine tolerances and repeatability. This lead to collaboration with Phillips Innovation Services via the EUMINAfab micro-nano fabrication scheme [32] whereby the structure fabrication was carried out at Philips, Eindhoven (based on LSBU designs and requirements) using commercial processes with high levels of accuracy and repeatability. This is described in Chapter 5

1.6. Thesis Layout

This thesis is laid out as follows:

A review of appropriate literature and a discussion of the current state of the art in the field are undertaken in Chapter 2 whilst Chapter 3 addresses the experimental and characterisation techniques utilised in the project.

Chapter 4 details the development of ancillary processes required for the fabrication of functioning electronic devices including metal and transparent conductive oxide contacts and edge isolation techniques.

The design, preparation and optical properties of the micro-rods are worthy of discussion independently of the ultimate purpose of device preparation. Chapter 5 details the modelling development undertaken to refine the parameters of the structures that were ultimately fabricated. It also includes results for the optical performance of the structures as well as the enhancement achieved by the application of anti-reflective coatings.

The formation of a functioning, shallow emitter by proximity rapid thermal diffusion was a major element of this project and occupies Chapter 6.

Chapter 7 addresses the fabrication and characterisation of micro-rod solar cells as well as covering the electronic enhancements of aluminium zinc oxide.

Finally, Chapter 8 includes conclusions and recommendations for future work.

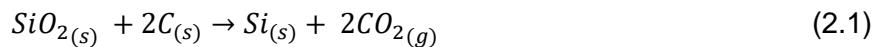
Chapter 2. Literature Review

This chapter will address the current state of the art in fields related to those that will be investigated by this project. It will also address semiconductor and device theory to provide a suitable understanding of the means by which photovoltaic devices operate.

2.1. Semiconductor Materials

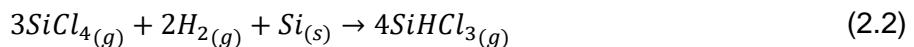
Solar cells are photovoltaic devices, that is, devices capable of directly converting the energy of incident photons into electrical energy. This effect occurs in semiconductor materials, of which Si, GaAs, CIGS, and CdTe are some common examples. Despite this variety of potential materials, at present, solar cells manufactured from single crystal silicon (Si) wafers dominate the PV industry. Whilst an oversimplification, this is essentially due to silicon being the second most common element in the earth's crust and that it can be straightforwardly refined from the abundant silicon dioxide (SiO_2).

Silicon wafers are prepared in a multi-step process, which starts with the production of metallurgical grade silicon (98-99% pure) from white quartzite sand (a form of silicon dioxide) [33]. This is heated in an arc furnace with carbon [34] producing silicon via the reaction:

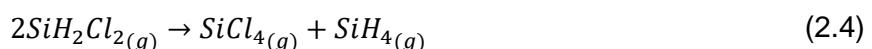
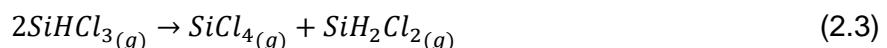


Before this silicon can be used to produce solar cells, it must be further refined to a purity approaching 99.9999% (6N) or alternatively to 99.9999999% (9N) if it were to be used in the semiconductor industry [34].

This is commonly achieved via the silane process [35] by heating the silicon to 500 °C at a pressure of 30MPa (to improve the reaction rate) in an environment of hydrogen (H_2) and tetrachlorosilane (SiCl_4) producing trichlorosilane (SiHCl_3) via the reaction:



The trichlorosilane is then reduced to dichlorosilane (SiH_2Cl_2) and tetrachlorosilane (which can be recycled), followed by the disproportionation of the dichlorosilane to silane and further tetrachlorosilane.



The final stage is the pyrolysis of silane at temperatures of 800-1000 °C producing high-purity silicon and hydrogen.



This is the same process that is used to deposit thin film silicon via Chemical Vapour Deposition (CVD), which is discussed in more detail later.

The silicon produced by this method is of polycrystalline formation. That is, silicon with crystalline formations on the order of millimetres or centimetres but without long range order like that of a single crystal silicon wafer [36].

To obtain single crystal silicon from the polycrystalline material it is melted in a crucible and a single crystal seed is lowered into the melt. As it is drawn out of the melt, the molten silicon seeds and solidifies forming a long cylindrical boule of single crystal material with dimensions dependant on the draw rate. By this method, boules of silicon with diameters up to 300 mm are achievable [37].

The silicon can be doped as necessary at this point by adding appropriate materials to the melt, i.e. phosphorus or boron. The solidified boule is then sliced and polished to produce wafers.

In this pure form, silicon has a diamond cubic crystalline structure with long range order. Each silicon atom forms four bonds to its nearest neighbour and the repetitive arrangement of this structure can be described by one of the Bravais lattices [38]. In the case of silicon the arrangement is of the cubic variety of which there are three bravais lattice arrangements; simple, body centred and face centred. Of these three, silicon occupies an additional subset described as diamond face centred. This describes an arrangement where every point and every face centre in a cubic cell is occupied by a silicon atom and additionally each of the points shares an additional silicon atom (Fig 1). The positional arrangement of the atoms is described by Miller indices [39].

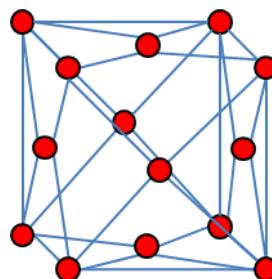


Fig 1. The diamond face centred arrangement of single crystal silicon atoms

2.2. Semiconductor Physics

To understand semiconductor operation, it is necessary to briefly consider Bohr's Model of the atom [40]. This describes an atom as a central nucleus formed of neutrons and protons with a nominally positive charge, around which resides a cloud of electrons with a nominally negative charge. The electrons are arranged in orbits with increasing energy levels the further away from the nucleus they are located. The energy levels are discrete and defined and electrons cannot reside elsewhere than at these various levels, as such they are referred to as allowed energy levels. When atoms are brought together in a solid, the individual electron energy levels combine to form energy bands. The outer most level containing electrons is referred to as the valance band and the electrons it contains referred to as valance electrons. Above the valance band exists a region called the forbidden band. This is not a literal gap in space but rather an energy gap of a defined value, which an electron in the valance band must possess in order to cross. Above this gap is the conduction band, which is the next energy level up from the valance band and is devoid of electrons. Any electrons reaching this empty level are free to take part in conduction, therefore the number of electrons in an atoms valance band and its band gap effectively define whether a material is a conductor, semiconductor or insulator.

Insulators have a very large band gap making conduction nominally impossible except under certain conditions. Conductors have overlapping valence and conduction bands or partially filled valance bands which allow the free flow of electrons and as a result current flow.

Semiconductors have variable band gaps whose value of E_g defines the energy in electron volts (eV) required for electrons to transition from the valence to conduction band [41]. Semiconductors at absolute zero ($0 \text{ } ^\circ\text{K}$) have full valance bands and empty conduction bands and the lack of thermal energy precludes the movement of electrons across the band gap. As a result, semiconductors at absolute zero behave as insulators.

The probability of an allowed energy level in a semiconductor being occupied by an electron is defined by the Fermi-Dirac Distribution Function [42]. This defines the probability $f(E)$ that an energy level E will be filled by an electron according to the equation:

$$f(E) = \frac{1}{1 + \exp((E - E_f)/(k_B T))} \quad (2.6)$$

Where k_B is Boltzmann's constant and T is the temperature of the semiconductor in Kelvin. E_f is referred to as the Fermi Energy Level and is defined as the point where the probability of an energy level being occupied by an electron is 0.5 or 50%.

It can be observed therefore that intrinsic semiconductors and insulators will have a Fermi Energy Level which lies midway between the valence and conduction bands, whilst in conductors it will lie at an allowed level.

2.3. Band Gap

Semiconductor materials are separated into two groups; direct and indirect band gap. A material is a direct band gap semiconductor if the electrons and the holes in the valence band and conduction band have the same momentum and can transition directly between the two when subjected to a photon of the same energy as the band gap (Fig 2a). A material that is an indirect band gap semiconductor requires that an electron excited by an incident photon also interact with a lattice vibration called a phonon to allow it to gain or dissipate momentum to match that of the holes in the conduction band [43] (Fig 2b). The requirement for this additional interaction makes indirect band gap semiconductors less efficient absorbers of light. Photons with energy less than that of the band gap (approx 1.1 eV for silicon) are unable to excite electron transitions and the semiconductor effectively becomes transparent to these wavelengths [44].

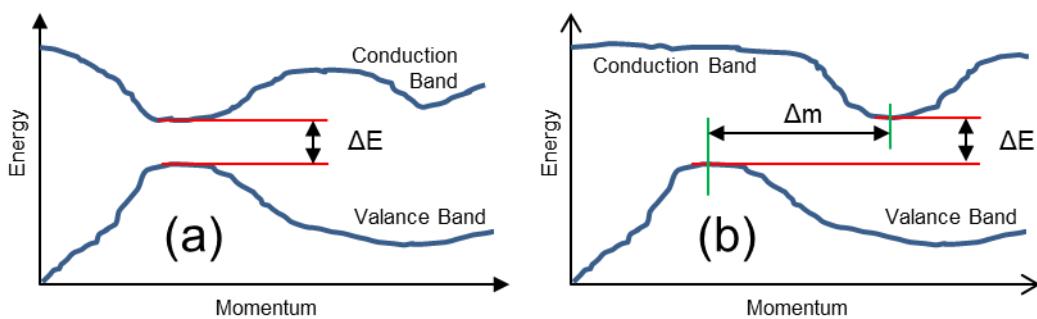


Fig 2. Band gap energy and momentum. In a direct band gap semiconductor (a), an electron excited by a photon with adequate energy (ΔE) may be promoted directly from valence to conduction band as they have equivalent momentum. In an indirect band gap semiconductor (b), the excited electron must also gain or lose momentum (Δm) by interacting with a lattice vibration called a phonon to cross the forbidden band. (Image based on [45])

2.4. Doping

Silicon has a crystal lattice formed of atoms with four covalent bonds. In this state it is described as intrinsic [46], that is with no significant dopant species incorporated into the

lattice (Fig 3a). To form a functioning solar cell requires doping silicon to modify the number of intrinsic electrons and holes.

P-type silicon has a deficit of electrons which are provided by incorporating a trivalent Group III element into the lattice (Fig 3b). Group III elements such as boron or gallium have three bonds which when incorporated into the silicon leave a dangling silicon bond and create a hole. N-type silicon on the other hand has an excess of electrons which come from a pentavalent Group V element. Group V elements such as phosphorous or arsenic form 4 covalent bonds, leaving an excess electron for each incorporated dopant atom (Fig 3c). It should be noted that despite the incorporation of extra holes or electrons into the lattice, the electrical neutrality of the lattice remains. This is because, for every additional mobile charge carrier, there is an immobile donor atom which possesses the opposite charge and maintains the neutrality of the crystal material.

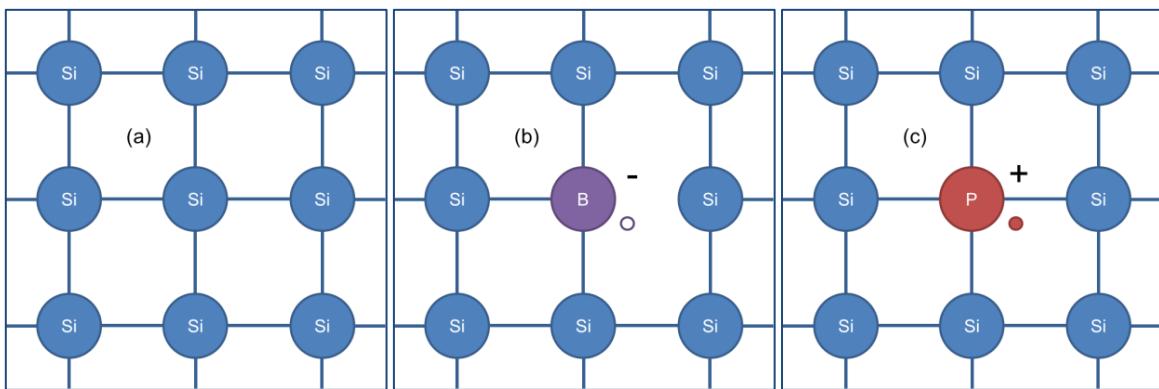


Fig 3. Incorporation of impurities into the silicon lattice. Intrinsic silicon (a) has four covalent bonds and is devoid of doping species. Incorporation of boron into the lattice (b) results in the creation of dangling silicon bond and the absence of an electron (i.e. a hole) with the resulting material referred to as p-type. Incorporation of phosphorus on the other hand leads to n-type silicon (c) with an excess bond in the lattice and an extra free electron.

2.5. The p-n Junction

The result of two oppositely doped layers of silicon in a structure is the formation of a p-n junction. Here, free electrons from the n-type layer diffuse across the junction to the p-type and the holes diffuse to the n-type due to the concentration gradients. This diffusion results in an area around the junction with many immobile ionised donor atoms and few mobile charge carriers. This area is described as the depletion or space charge region [47] (seen extending from $-x_p$ to x_n in Fig 4). The depletion region ends up with a net positive charge on the side with a build-up of donors in the lattice (immobile atoms short of an electron) and a

negative charge on the side with an excess of acceptors (immobile atoms short of a hole) on the opposite side.

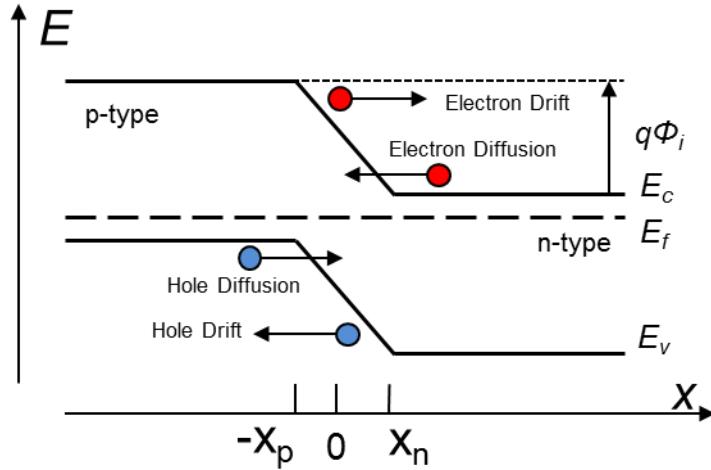


Fig 4. The band diagram of a p-n junction in silicon. E_c , E_f , E_v and $q\phi_i$ represent the energy of the bottom of the conduction band, the Fermi level, the top of the valance band and the built in field respectively. Mobile carriers (holes in p-type and electrons in n-type) diffuse from areas of high concentration into those with a lower concentration. Meanwhile, the resulting electric field resulting around the depletion region causes some mobile carriers to drift in the opposite direction. These processes continue until the two mechanisms cancel each other out and equilibrium is reached. (Image based on [48])

The resulting electric field that is present in the cell when unbiased in turn causes carriers to drift in the opposite direction to diffusion. These processes continue until diffusion and drift balance and inhibit further carrier diffusion. The electric field at equilibrium is described as the built in electric field or contact potential [43], referred to as ϕ_i and described by:

$$\phi_i = V_t \ln \frac{N_d N_a}{n_i^2} \quad (2.7)$$

Where V_t is the thermal voltage (0.0259 V at 25 °C) and N_d , N_a and N_i are the number of donor, acceptor and intrinsic atoms respectively. This equation essentially quantifies the sum of the bulk electrical potentials in each region resulting from the incorporation of the donor and acceptor atoms.

It can be seen from Fig 5 that by applying a voltage bias, V_a , to the junction it is possible to increase or decrease the potential across the junction and the width of the depletion region. In reverse bias the potential across the junction is increased with a corresponding increase

in the depletion region width. In forward bias the potential is reduced with a corresponding decrease in the width of the depletion region. This variation in the barrier height increases or decreases the likelihood of carriers diffusing across the junction and in turn whether or not conduction in the semiconductor is able to occur.

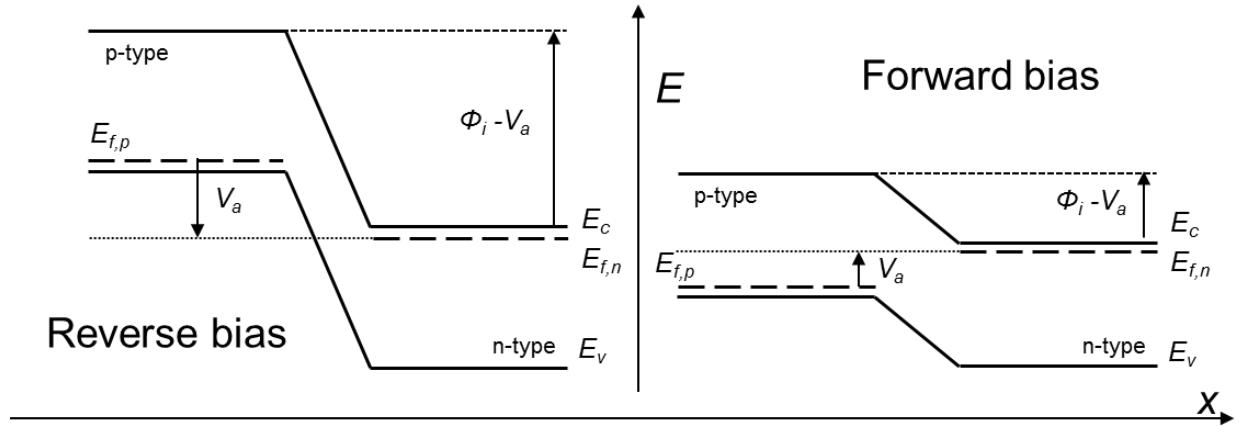


Fig 5. The effect of biasing a p-n junction in silicon. E_c , $E_{f,n}$, $E_{f,p}$, E_v and ϕ_i represent the conduction band, the Fermi level in the n-type region, the Fermi level in the p-type region, the valance band and the built in field respectively. Under reverse bias ($-V_a$) the potential across the semiconductor is increased ($\phi_i - (-V_a)$) along with the width of the depletion region. Forward bias (V_a) leads to a reduction in the potential ($\phi_i - V_a$) and associated reduction in the depletion region width. (Image based on [49])

Under dark conditions a solar cell exhibits diode like behaviour and its properties are dependent on biasing. However, when exposed to incident photons whose energy is at or above the band gap energy of the semiconductor, electrons can be excited to the conduction band and generation may take place.

2.6. The p-n Junction under Illumination

The generation of charge carriers in a p-n junction device is dependent on the absorption of photons within the semiconductor material. The absorption rate of light within the material is proportional to the intensity remaining at a given depth. This can be described by the exponential relationship:

$$F_x = F_{x,0} \exp(-\alpha_\lambda(x - x_0)) \quad (2.8)$$

where F_x is the number of photons at point x ; $F_{x,0}$ is the number of photons on the surface where $x = 0$; and α_λ is the absorption coefficient which is itself dependant on the wavelength of light [50].

Where the energy of a photon is greater than that of the band gap of the illuminated semiconductor, absorption will occur and result in the production of minority carriers (electrons in the p-type and holes in the n-type). Unless the energy of the photon is identical to that of the bandgap, the promoted carriers will be raised to a higher energy level before falling back with the excess energy being dissipated by thermalisation into the lattice.

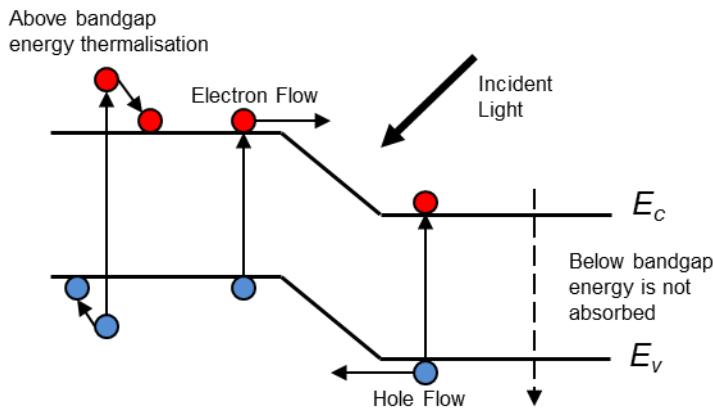


Fig 6. The carrier generation mechanism in silicon under illumination. Photons with energy greater than that of the band gap can create minority carriers which are swept across the junction and form the solar cell current. Photons with energy lower than that of the band gap are not absorbed and pass through without generating carriers. (Image based on [51])

The carriers diffuse through the bulk material where upon reaching the junction they are swept across by the electric field (Fig 6). These light generated carriers form the solar cell current.

2.7. Lifetime and Recombination

The existence of minority carriers is contingent on the minority carrier lifetime of the material which is itself dependant on recombination mechanisms. Materials with longer carrier lifetimes will generally give better performance as the chance of carriers reaching the junction is greater. Carrier combination mechanisms include radiative, auger and Shockley-Read-Hall.

Radiative recombination is the dominant recombination mechanism in direct bandgap semiconductors and is essentially the reverse of the carrier generation mechanism [52]. Its

effect on indirect band gap semiconductors such as silicon is extremely low and normally neglected.

Auger recombination requires three carriers and dominates in high doping concentration semiconductors. An electron and hole recombine but rather than emitting the energy as thermal energy into the lattice or as a photon, the energy is transferred to a third carrier consisting of an electron residing in the conduction band [53]. This electron then returns to the conduction band edge by dissipating the energy thermally into the lattice. In heavily doped silicon, auger recombination is responsible for limiting carrier lifetime and ultimate efficiency [54].

Recombination through defects, also referred to as Shockley-Read-Hall or SRH recombination [55][56], does not occur in pure material without defects. Single crystal silicon therefore does not suffer significantly from this type of recombination. However, high levels of doping can cause lattice defects which permit SRH recombination to occur. The recombination process occurs in two stages; first an electron (or hole) is captured in a trap level within the forbidden region. Second, if a hole (or electron) moves into the same occupied energy state before the trapped carrier can be thermally promoted to the conduction band it will recombine.

Taking into account the aforementioned forms of recombination, the bulk lifetime of carriers in a material can be described by:

$$\frac{1}{\tau_b} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_A} + \frac{1}{\tau_{SRH}} \quad (2.9)$$

where τ_b is the bulk, τ_{rad} is the radiative, τ_A is the Auger and τ_{SRH} is the Shockley Read Hall lifetime, respectively.

Whilst these types of recombination have a substantial effect on semiconductor device performance, another significant source of loss is that which occurs at the surface of materials referred to as surface recombination [57]. Surfaces typically contain a large number of recombination sites because of the abrupt end of the semiconductor material which results in many electrically active states [58]. Furthermore, the surface of the device is likely to suffer from additional impurity based defect sites as it is exposed during processing. Commonly employed means to reduce recombination include passivation annealing in hydrogen gas [59] which bonds with exposed defect sites and growth of oxide or nitride layers [60] which utilise a similar mechanism.

2.8. Cell Characterisation and Efficiency

Solar cell performance is commonly assessed by current-voltage (I-V) analysis whereby the device is biased by a voltage source and the resulting current flow measured. This is typically done using a sourcemeter which is capable of both supplying and measuring voltage and current in a single device.

The I-V characteristics of a solar cell under dark conditions are nominally similar to a conventional diode. Dark I-V measurements are taken by biasing the device to cause carrier injection, which nominally replaces the light generated carriers produced when the cell is under illumination.

Fig 7 shows a typical dark current sweep (purple) in the 1st quadrant where the device is sourcing current from the sourcemeter and a sweep under illuminated conditions (red) with the curve shifted into the 4th quadrant as the sourcemeter sinks the light generated current produced by the cell. In an ideal cell, the two curves are identical and are simply shifted by the magnitude of the light generated current, however, in the real world resistive effects and recombination prevent this being the case.

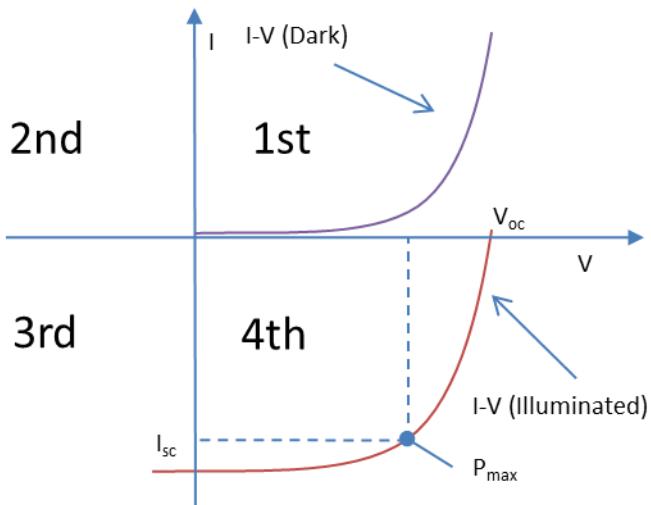


Fig 7. Simplified I-V curves showing the measured current-voltage profile of a solar cell under dark and illuminated conditions. Highlighted are the open circuit voltage (V_{oc}), short circuit current (I_{sc}) and maximum power (P_{max}) points.

If the cell is short circuited there is no voltage potential and the maximum cell current or short circuit current (I_{sc}) is produced according to:

$$I_{sc} = -I_L \quad (2.10)$$

where I_L is maximum light generated current. Conversely if the cell is open circuit, no current flows and the resulting potential is defined as the open circuit voltage (V_{oc}) given by:

$$V_{oc} = \frac{kT}{q} \ln \left(\frac{I_L}{J_0} + 1 \right) \quad (2.11)$$

Where J_0 is the device saturation current which depends on the recombination rate, k is Boltzmann's constant, T the temperature in Kelvin and q the charge of an electron.

The maximum power (P_{max}) produced by the cell occurs at the convergence of maximum current (I_{max}) and maximum voltage (V_{max}), usually around the knee of the I-V curve.

Cell efficiency η is calculated by:

$$\eta = \frac{P_{max}}{P_{opt}} \quad (2.12)$$

Where P_{max} is maximum electrical power and P_{opt} is total optical flux falling on the cell.

The fill factor of a cell is the ratio of maximum obtainable power to the product of the open circuit voltage and short circuit current. It is given by:

$$FF = \frac{P_{max}}{V_{oc} I_{sc}} \quad (2.13)$$

There are a variety of factors which can affect the performance of a PV device. Considering the equivalent circuit or diode model of a solar cell (Fig 8) allows these to be identified.

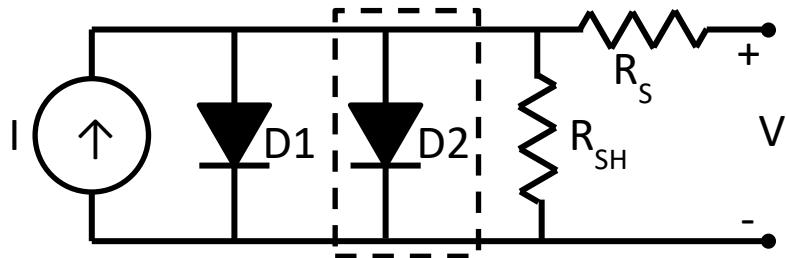


Fig 8. Solar Cell Equivalent Circuit (diode model). Shown are both the single (diode D1 only) and double diode (diode D1 and D2) variants. The second diode accounts for the variable location of recombination of the device and the effect this has on the ideality factor.

The diode model of a solar cell describes a photovoltaic device in electronic circuit form with a combination of resistances and either one or two diodes if the single or double diode model is considered [61].

The simpler single diode model assumes a constant value for the diode ideality factor. The ideality factor describes how closely the behaviour of a diode is to the ideal diode equation [62], given below.

$$I = I_L - I_0 \left[e^{\left(\frac{qV}{nkT} \right)} - 1 \right] \quad (2.14)$$

Where I is the current flowing through the diode, I_0 is the dark saturation current, V is the voltage across the device, q is the charge on an electron, k is Boltzmann's constant, T is the temperature in Kelvin and n is the ideality factor. The dark saturation current results from minority carrier diffusion into the depletion region [63]. It is generally independent from the reverse bias applied to the device but affected by temperature and material quality.

This equation makes certain simplistic assumptions, whilst in practice there are other factors which prevent real devices following it. The ideality factor describes the extent of the effect of these factors. The ideal diode equation is predicated on all recombination occurring by band to band transitions or trap levels within the bulk of the device rather than the junction. These assumptions produce the derived equation given, with an ideality factor, n that is equal to one.

In reality, recombination occurs due to a variety of other methods and in other regions of the device and the result of this are ideality factors which deviate from one. One of the most significant effects on the ideality factor is the voltage present across the device. At higher voltages, where the recombination is dominated by surface effects and occurs predominantly in the bulk region, the value of n is indeed close to one. However, at lower voltages, the junction recombination dominates and the value for n approaches two. To account for this, a second diode is added to the model in parallel with the existing with n typically set equal to two [62]. In a similar fashion, the dark saturation current is dependent on the operating voltage, with I_{01} describing the dark current at higher voltages predominantly resulting from the bulk region and I_{02} describing the dark current at lower voltages predominantly resulting from the depletion region.

$$I = I_L - I_{01} \left[e^{\left(\frac{q(V-IR_s)}{kT} \right)} - 1 \right] + I_{02} \left[e^{\left(\frac{q(V-IR_s)}{2kT} \right)} - 1 \right] + \frac{V - IR_s}{R_{shunt}} \quad (2.15)$$

In addition to diodes in the cell equivalent circuit there are two resistances, one in series and one in parallel, referred to as the series and shunt resistances respectively. The series resistance accounts for bulk, emitter and contact resistance in the device with smaller values being better [64]. The shunt resistance describes short circuit or leakage paths through the device which interfere with the diode like operation and cause efficiency losses, accordingly higher resistance values are better [65]. Both shunt and series resistances are of particular concern in the case of junctions prepared on micro and nano scale devices as emitters are generally thin and can exhibit both high resistance and the risk of non-uniformity with the associated possibility of shunt paths.

It is possible to estimate the values of shunt and series resistance directly from a measured I-V curve as each has a characteristic effect on the shape of the plot. The shunt resistance can be estimated by finding the slope of the I-V curve at the short circuit current point [66]. In a similar fashion finding the slope of the I-V curve at the V_{oc} can approximate the series resistance. This method is not without its inaccuracies but it permits straightforward initial analysis of a device's performance [67].

2.9. Quantum Efficiency

The term quantum efficiency (QE) as applied to photosensitive devices defines the ratio of incident photons to converted electrons (IPCE) [68]. The QE of a PV device is generally measured over a wide wavelength range as this allows the efficiency of charge carrier generation at given photon energies to be assessed. There are two types of quantum efficiency to be considered; external (EQE) and internal (IQE).

EQE is the ratio of generated charge carriers to incident light falling on the cell whilst IQE is the ratio of generated charge carriers to incident light that is absorbed by the cell. The IQE is therefore always larger than the EQE with a poor IQE indicating that the cell is not efficiently converting photons to charge carriers. To calculate the IQE of a device, one first measures the EQE and then the reflection (R) and transmission (T) of the device and then combines the data according to:

$$IQE = \frac{\text{electrons/s}}{\text{absorbed photons/s}} = \frac{EQE}{1 - R - T} \quad (2.16)$$

Fig 9 shows a typical QE curve for a silicon solar cell and the ideal QE profile for a perfect device. It is possible by analysing the QE curve to assess the loss mechanisms affecting device performance. For example, passivation at the front of the cell affects carrier generation near the surface which results from short wavelength light and accordingly

reduced short wavelength QE is indicative of high front surface recombination. Similarly mid-wavelength QE and long-wavelength QE are indicative of the device's bulk and rear surface recombination rates respectively.

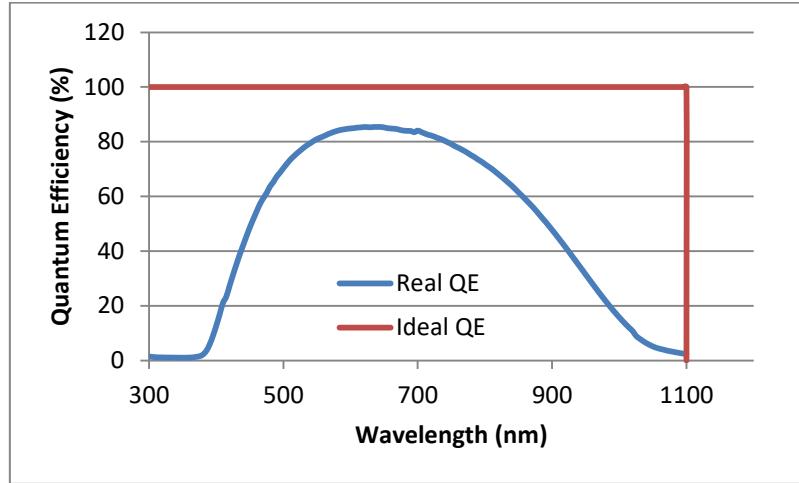


Fig 9. Real and ideal QE profiles for a silicon solar cell. The real profile highlights the greatest conversion efficiency in the middle wavelength range and the challenges of poor conversion at the longer and shorter wavelengths.

The real QE data shown in Fig 9 is for a highly doped emitter which despite excellent surface passivation still suffers from high front surface recombination. As is discussed later in this chapter, structured solar devices are reliant on highly doped emitters for good performance and therefore careful monitoring of QE will be important for optimising device performance.

2.10. Solar Cell Design

This section will discuss the development of planar based solar devices and the current state of the art for the various technologies.

2.10.1. Planar Cells

The traditional silicon wafer solar cell is based on well-established planar junction technology and combined with various enhancements to optimise performance.

Typical silicon wafers for PV purposes are in the order of 200-300 microns thick and, with the aid of anti-reflection coatings on the front surface and a back surface reflector on the rear, are able to trap and absorb adequate light to produce average panel conversion efficiencies on the order of 16% to 18% [69]. The record for a planar silicon solar cell (25%) was held for a prolonged period by the Passivated Emitter, Rear Locally diffused (PERL) cell (Fig 10) developed by the University of New South Wales (UNSW) [70].

The bulk of the cell is made up of the p-type monocrystalline wafer upon which the cell is based. Prior to emitter formation an SiO_2 mask is deposited atop the wafer and patterned using photolithography, then the inverted pyramids are etched utilising a hot potassium hydroxide (KOH) solution. Following this, boron diffusion is carried out through an oxide mask on the rear side of the device to form a back surface field (BSF). Next, multiple oxide mask, etching and diffusion steps are carried out to form first the n-type emitter and then the n+ selective emitter [71]. Prior to contact formation, SiO_2 is grown on both sides of the device to passivate the exposed silicon surfaces, followed by additional etching steps to open the oxide in the necessary contacting locations. Aluminium is then deposited on the rear side to contact the p-type material whilst the Ti-Pd-Ag grid is deposited through windows opened in the front oxide to contact the n+ selective emitter. Finally the whole device is subjected to an annealing step to sinter the metal layers and form ohmic contacts.

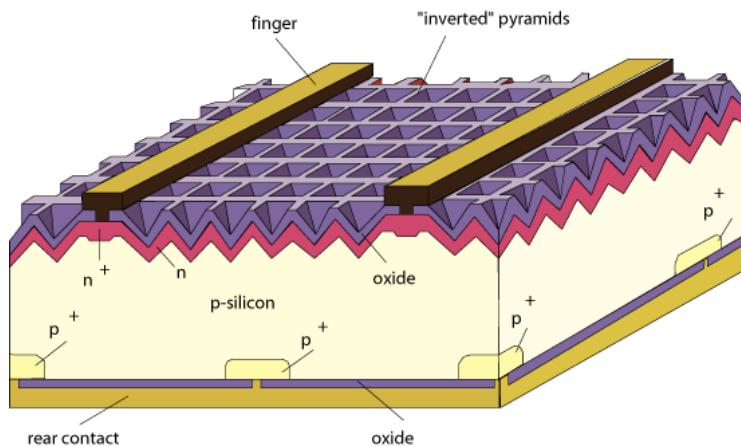


Fig 10. PERL silicon solar cell cross section. Shown is the p-type silicon base wafer with selectively doped emitter for optimum contacting, oxide layers for anti-reflection and passivation and the inverted pyramid anti-reflection scheme. [70]

2.10.2. HIT Cells

The Panasonic (formerly Sanyo) HIT cell (Heterojunction with intrinsic thin layer) is a heterojunction design based on an n-type wafer but with an amorphous silicon emitter. Amorphous silicon (a-Si) is a non-crystalline allotrope of silicon without the long range crystallographic order present in its single crystal form [72].

The HIT cell structure (Fig 11) consists an n-type wafer as the substrate, atop this is deposited an intrinsic (i-layer) of amorphous silicon and then the p-type amorphous emitter. On the rear side of the wafer another intrinsic layer is deposited followed by an n-type amorphous emitter. The intrinsic layers are an important component of the cell design as they keep the dopant materials separate and limit the defects caused by these [73]. The

front surface has an additional layer consisting of a transparent conductive oxide (TCO) which allows current collection over the full surface without shading the device. Growing amorphous layers on silicon requires lower temperature processing than epitaxial growth resulting in reduced manufacturing costs [74].

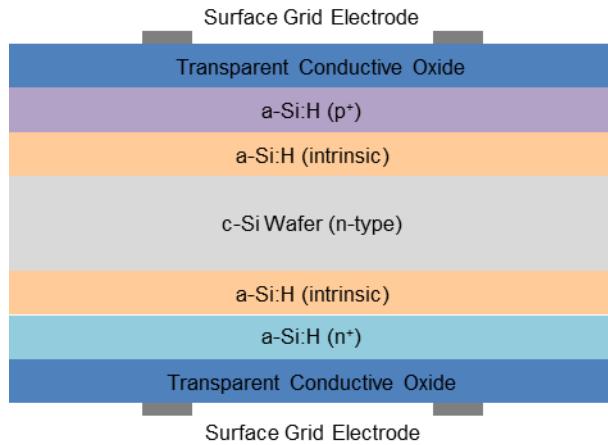


Fig 11. HIT silicon solar cell cross section. Shown are the n-type silicon base wafer sandwiched between the intrinsic and heavily doped amorphous layers and top and bottom transparent conductive oxide contacts.

Utilising this design and other enhancements, including excellent passivation at the heterointerface, peak efficiencies of 25.6% have been achieved [75]. This efficiency, achieved in 2014, set a new absolute efficiency record for a single junction crystalline silicon solar cell. The other key advantage of this arrangement is the ability to produce very high values for V_{oc} with voltages in excess of 710 mV being demonstrated [76].

2.10.3. Interdigitated Back Contact (IBC) Cells

The concept of the interdigitated back contact (IBC) device (Fig 12) was first proposed by Lammert and Schwartz [77] in 1977. IBC solar cells reduce efficiency losses resulting from front contact shading. They achieve this by placing both p+ and n+ doped regions on the rear side of the device eliminating the requirement for front contacts. This arrangement necessitates a thin cell produced from very high quality material to ensure high minority carrier lifetimes which permits electron-hole pairs generated at the front surface to reach the back of the cell and be collected. Low resistance contacts are important to minimise series resistance losses and passivation of the front and rear surfaces reduces surface recombination. The first practical IBC device based on the proposed design was fabricated by Swanson with recorded efficiencies of 23% efficiency at 200x solar concentration and 24 °C operating temperature [78].

Due to their design, these devices are commonly found in concentrator photovoltaic systems. At the time of writing, the most efficient IBC concentrator cell is by Amonix at 27.6% under 92 Suns illumination whilst the highest efficiency module, also by Amonix, is a triple junction device under 1092 Suns for 35.9% efficiency [79]. On a domestic level, Sunpower produce their single junction Maxeon range with cell efficiencies of 24% and modules with conversion efficiency in excess of 20% [80].

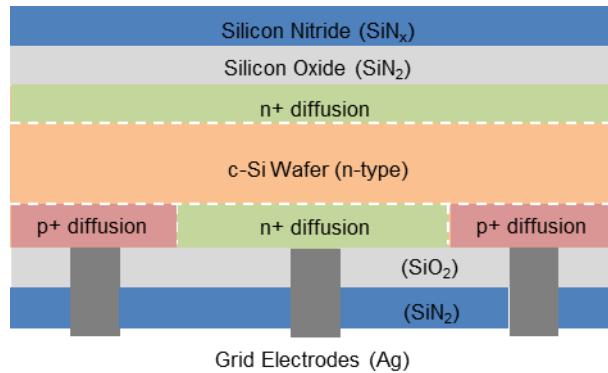


Fig 12. IBC silicon cell cross section. Shown are the selectively doped regions at the rear for contacting and the multi oxide layer passivation and anti-reflection schemes on both front and rear of the device.

2.10.4. Amorphous Silicon Thin Film Solar Cells

As was briefly mentioned earlier in this chapter, it is possible to deposit silicon directly from the gas phase from a feedstock gas such as silane. Doing so removes the requirement for the complex processing required to produce poly or mono crystalline silicon.

One of the earliest examples of this was work undertaken by Chittick, Alexander and Sterling in 1968 [81]. They demonstrated deposition of an amorphous silicon (a-Si) film from silane by radio-frequency glow discharge and noted that the deposited films demonstrated a photoconductive effect. Silicon in its amorphous form demonstrates no long range crystal order and, of interest from a solar point of view, is a direct-bandgap semiconductor [82].

A key difficulty with amorphous silicon, arising from its non-crystalline formation, is the large number of dangling bonds that exist in its structure. These cause a number of problems from an electronic point of view which made fabrication of solar cells challenging. In 1975 Spear and Le Comber demonstrated deposition of amorphous silicon by glow discharge with the addition of hydrogen [83]. The hydrogen occupies the dangling atomic bonds in the amorphous silicon structure effectively passivating them and producing hydrogenated amorphous silicon (a-Si:H). In the same work, they demonstrated the ability to substitutionally dope the deposited silicon by the addition of small quantities of diborane or phosphine. This

was a significant achievement as, until this point, doping of disordered materials such as a-Si had been thought impossible due to the 8-N Mott's rule [84]. This stated that all elements introduced into such materials would be bonded in their configuration and unable to act as donors or acceptors.

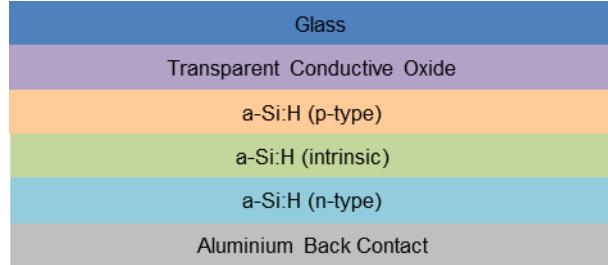


Fig 13. Amorphous silicon solar cell structure. Shown is the superstrate configuration whereby the various cells layers are grown on the glass layer and then the device is inverted to operate. [85]

Work on fabricating an a-Si solar cell (Fig 13) had begun as early as 1974 when Fuhs, Niemann and Stuke at RCA laboratories produced an a-Si on single crystal wafer device and observed its rectifying properties [86]. However, it was not until 1976 that Carlson and Wronski developed the first device that could fully be described as a thin film a-Si solar cell [87], which demonstrated 2.4% efficiency under AM1 illumination.

Efficiencies were progressively improved until 1997 when United Solar Systems Corporation demonstrated a 13.0% stable efficiency triple junction a-Si solar cell [88]. This is approaching the efficiency limit of 14-15% predicted by Carlson and Wronski. It is also the highest efficiency device based solely on a-Si.

Since 1997 the best amorphous efficiency has risen only slightly with the record as of 2015 being 13.6% held by AIST with their triple junction a-Si:H/μc-Si:H/μc-Si:H device. This configuration is based on the micromorph concept, first proposed by Meier et al in 1995 [89]. This combines amorphous and microcrystalline films in a tandem structure, taking advantage of their differing band gaps to absorb a greater range of the solar spectrum.

2.11. Surface Structured Cells

The solar cells discussed in the previous section all share a common design feature, that of a planar junction which is perpendicular to the direction of incident solar radiation. This necessitates a relatively large thickness of material for an indirect bandgap semiconductor like silicon to efficiently absorb the incident light [90]. The result of this is wafer based solar cells with absorber thickness of 200-300 μm coupled with anti-reflection schemes to achieve

useful light harvesting [91]. This significant quantity of material also means that carriers generated deep in the base wafer must diffuse relatively large distances to reach the junction, necessitating high minority carrier lifetimes [92]. Long lifetimes in turn require high quality silicon, adding further demands to the list of requirements for efficient wafer based solar cells.

If the absorption medium is placed at right angles to the junction, such as in a radial p-n junction design, the optical absorption distance and the minority carrier diffusion length are decoupled (Fig 14).

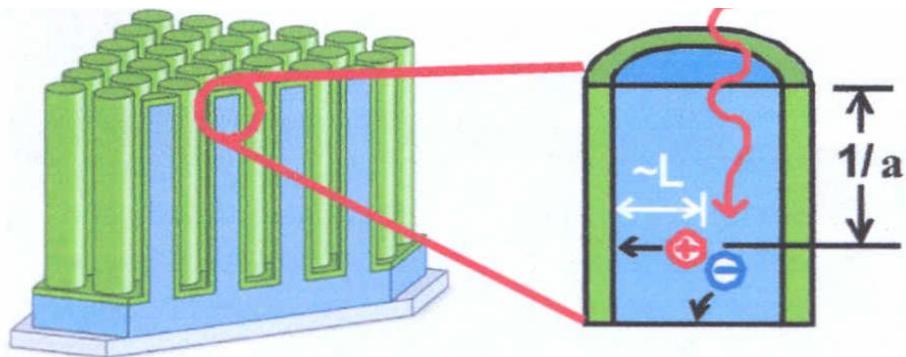


Fig 14. Simplified cross sectional diagram of a radial p-n junction. This highlights the vertical photon absorption and horizontal carrier collection and demonstrates the decoupling of the two distances. [93]

By reducing the distance that carriers must diffuse to reach the junction the requirement for very high purity silicon is relaxed and the overall material requirement may be reduced [94].

There are two key elements to the design and fabrication of a structured solar cell. The first is the design of the array for best optical performance and the second is the preparation of the electronic element of the device. Unfortunately it is often the case that the best-case design for each element contraindicates that of the other [95]. Initially this review will consider each element independently before investigating the necessary compromises to optimise a complete device.

2.12. Optical Performance Modelling

Whilst there is a wide array of designs and configurations that have been investigated for light trapping, the focus of this review will be on cylindrical pillar like structures of nanometre and micron scale.

In their paper [96], L. Hu and G. Chen investigated nanowire structures in the range of 50 nm – 80 nm diameter with a periodicity of 100nm by transfer matrix methods (TMM) simulation [97]. They selected wire lengths of 1.16 μm , 2.33 μm and 4.66 μm to show the effect of thickness dependant absorption, as these are values similar to the typical thickness of a thin film silicon device. The 1.16 μm length pillar devices exhibited inferior absorption in the longer wavelength region (450 nm to the bandgap at 1100 nm) to an equivalent 2.33 μm planar thin film. This results from the reduced density of the wires compared to bulk silicon and limited phonon interactions necessary for photon absorption in silicon. The range over which inferior absorption was observed reduced to 495 nm - 1100 nm for the longest modelled wires. It is to be noted that the wires exhibited superior anti-reflection to the thin film across the total examined wavelength, highlighting that the limiting factor for a wire only device is absorption related.

This was highlighted when the packing fraction was varied for a constant inter-wire spacing (i.e. the pillar diameter was modified). As the pillar diameter increased from 50 nm to 80 nm the peak absorption at the shorter wavelengths dropped and the bulk absorbance was red-shifted progressively to the longer wavelength region. The increasing wire diameter did result in greater reflection, however, it was noted that the increased long wavelength absorption would to some extent counteract the losses at the shorter wavelengths. The overall absorption efficiency of the various diameter wires was calculated and found to rise from 5.8% to 12.5% when increasing the wire diameters from 50 nm to 80 nm compared to 15.5% for the planar thin film. Thus the total absorption for a wire only device can be found to approach that of a thin film device with the limiting factor being the absorption above ≈ 440 nm.

Discussion to this point has been for structured devices where the simulated light fall is at a normal angle of incidence to the array. This is of course an unrealistic consideration when applying structures to a real world device and as such consideration should be made regarding this variable. Hu and Chen applied a variable angle of incidence to their wire model and found it to have only a minor effect on the absorbance. N. Lagos, M.M. Sigalas and D. Niarchos [98] agreed with this assessment in their paper, this time for wires in the region of 400 nm – 600 nm and slightly larger values for array periodicity. It is of relevance that the array absorption is nominally independent of incident angle as this is clearly important for real world considerations.

J. Li et al [99], whilst concurring that whilst the problem of longer wavelength absorption could be partially resolved with larger wire diameters, posited that the main limiting factor was the small periodicity (100nm). They investigated arrays of periodic wires by full wave

finite element analysis [100] with wire diameter (D) being a function of the periodicity (P) in the form D/P . A wire length of 5 μm was set and an equivalent thickness thin film of silicon used as a comparison for absorption, transmission and reflection. It was observed that as P was increased for a D/P of 0.5, the absorption edge shifts progressively towards the longer wavelengths due to the reduction in transmission. This results from the increased wire diameter enhancing longer wavelength light propagation and trapping within the array where the longer wavelengths would previously have easily passed through the short periodicity array. It was also noted that if P is excessively large then the incident light of shorter wavelengths will simply pass through the array without interacting. In this case the previously observed strong short wavelength absorption will be lost, resultantly an upper boundary condition for periodicity is created.

It was shown that it is necessary for the periodicity to increase proportionally with wire diameter, otherwise for a fixed P and an increasing D the transmission losses would fall but reflection losses would rise. To investigate the potential efficiency and corresponding D/P ratio, arrays of wires with P between 300 nm and 900 nm were modelled. For all values of P the peak efficiency was observed for a D/P value of 0.8. Furthermore, it was possible for a wide range of values of P (250 nm to 1200nm) to exceed the efficiency of a thin film silicon cell with thickness equivalent to wire length whilst using less overall material.

Li, Yu and Li [101] developed this modelling process further to investigate the effect of pillar length on ultimate efficiency. Selecting their optimal array periodicity of 600 nm and pillar diameter of 500 nm (giving a D/P value of 0.833) they modelled the ultimate efficiency (UE) of wires with length (L) 100 nm to 6000 nm. Ultimate efficiency was defined as the photoelectric conversion capability, where each photon with energy greater than the band gap and trapped by the device is converted into an electron-hole pair and extracted as electrical energy.

For wires with length less than 1000 nm the UE rose monotonically and notably exceeded a modelled 2000 nm thick film silicon device for a value of $L=400$ nm. Above 1000 nm, oscillation in the UE was observed. The potential loses for certain wire lengths were significant with L values of 1250 nm and 2500 nm showing losses of nearly 2% compared to the previous peak value before the UE recovered. Above $L=3000$ nm the UE enhancement began to saturate for a peak value of about 28% efficiency.

The authors noted that waveguide modes which are exhibited in the modelling, and provide some of the observed enhancement, result from near perfect structural uniformity exhibited by the model which is unlikely to be replicated by any real world fabrication technique. As a result the scattering-induced enhancement resulting from optimised wire spacing is the

primary factor to be considered when considering wire geometries and waveguide mode-induced enhancement may be neglected.

Also of note is the investigation into the effect of arranging the wires in a square or hexagonal array. It was found that provided arrays had identical configurations, i.e. periodicity, wire diameter and length, the resulting light trapping performance was very similar with hexagonal arrays demonstrating slightly higher values for UE.

Z. Duan et al [102] investigated similar parameters from the point of view of reflectivity of photon flux (RPF) calculated based on the array parameters by the transfer matrix methods. Unlike the previous models, however, they based their nano-rod arrays on a silicon base of semi-infinite thickness. This reduced the possible interactions of incident photons to either reflection or absorption with the assumption that all absorbed photons generated electron-hole pairs. This configuration more accurately reflects a potential real world configuration of a rod device where structures would either be grown onto or etched into a silicon wafer. Clearly, of course, the assumption that all absorbed photons generate carriers is unrealistic but does provide a useful maxima performance value. Unlike previous work which looked predominantly at the effect of array periodicity on optical performance, they considered the effect of the density of the array in pillars/cm² calculated from the period length and pillar radius.

It has been established thus far that the ratio of rod diameter (D) to period length (L) has a significant effect on photon absorption and will resultantly affect quantum efficiency (QE). To investigate this in more detail, the effect of D/L on rods with density 1×10^{10} pillars/cm² and of different lengths was modelled with the maxima QE for all lengths found to lay in the range 0.59 and 0.81. The peak value was found to be 0.72 for 0.09 μm height pillars which is slightly lower than the typical value of ≈0.8 from [99] but lays centrally between this and lower values (0.6) found in other work [103]. Notably, however, this peak value is for substantially shorter pillars than previous papers (90 nm vs >1 μm). At this optimum value, the peak QE is found to be 92.4%. Above this length the value falls to a stable plateau value of ≈84.4% indicating that greater pillar length does not result in substantially greater reflection but nor does it improve efficiency. This is in agreement with H. Wang et al [104].

With regard to the pillar density, it was observed that increasing the pillar density does not result in a reduction in reflection. This agrees with previous papers [105] where increased pillar density for the optimal diameter resulted in high reflection from the front surface of the structures. It was further found that for the optimum rod height and providing the optimum

ratio of 0.72 is maintained for a given diameter (and therefore density), the peak QE of 92.4% is always achieved.

It was also shown that the parameters are equally applicable to hexagonal arrays with the addendum that the optimum ratio for D/L falls to 0.67. This is in agreement with the value found by Li, Yu and Li for their hexagonal wire arrays and confirms their analysis that the arrangement of the wires or rods be they square or hexagonal, has a minimal effect on the performance of the array.

All of the models investigated thus far have assumed periodic arrays of structures with perfect organization. Whilst this reflects the case for this body of work it is worth briefly considering whether any benefit is gain from an element of random organization. Lagos et al [98] investigated disorder in three elements of their model; wire position in the array, the wire radius and the orientation of the wire relative to the surface. The disorder in the location of the wires in the array was found to have a minimal effect on the absorption of light whilst variable wire diameter was shown to improve the absorption at the shorter wavelengths. Disorder in the orientation of the wires had the largest effect although it was mostly negative with significantly reduced absorption for any considerable variation from vertical. This is in agreement with the work of Bao and Ruan [106] whose model concurred the substantial improvement from random diameter wires but with little effect from random position.

2.13. Device Performance Modelling

The concept of a radial junction solar cell with rod shaped structures was first explored from a device physics point of view by Kayes [93] in a comparison between the theoretical performance of equivalent planar and radial junction devices. The devices were modelled as p-type substrate with an n-type emitter or shell (see Fig 15) and the incident light was modelled as falling at a normal incidence to the surface. Of interest is the assumption that recombination in the devices was purely from Shockley-Read-Hall recombination with Auger recombination neglected. Resultantly modelled doping densities were limited to those unaffected by this form of recombination. This is notable as later in the paper it is observed that rod cells favour high doping densities which are known to be substantially affected by Auger recombination [107].

The parameters considered were cell thickness/rod length, doping density and material quality in the form of minority-electron diffusion length. The model assumed a 100% packing fraction for the rods so enhancement due to light trapping resulting from the structures was not considered. Two variations of the model were prepared, one where the trap density in

the device was constant throughout and the other where the trap density in the depletion region was decoupled from that in the quasineutral regions.

The J-V behaviour of modelled devices was described by the derived equation:

$$J = (J_{p_0}^p + J_{n_0}^n)(e^{qV/kT} - 1) - J_{p_l}^p - J_{n_l}^n - J_{g(V)}^{dep,p} - J_{g(V)}^{dep,n} + J_{r(V)}^{dep} \quad (2.17)$$

where $J_{p_0}^p$ and $J_{n_0}^n$ describe the dark saturation current in the p and n regions, $J_{p_l}^p$ and $J_{n_l}^n$ are the current density in the p and n quasineutral device regions, $J_{g(V)}^{dep,p}$ and $J_{g(V)}^{dep,n}$ are the light generated currents in the depletion regions of the p-type and n-type and $J_{r(V)}^{dep}$ is the recombination current density in the depletion region.

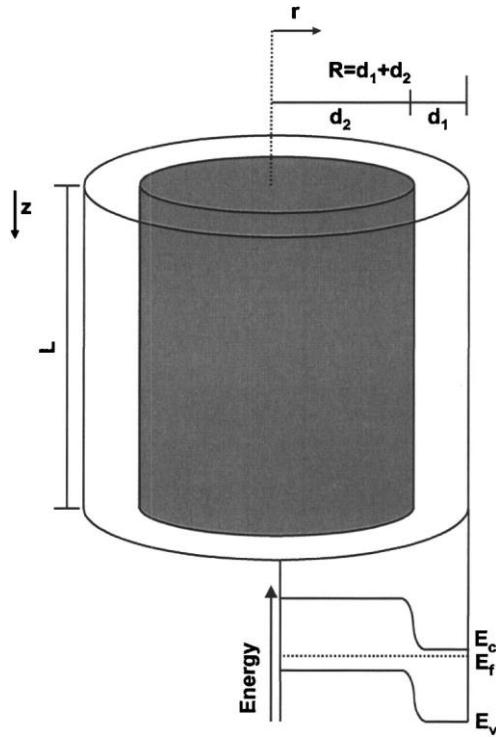


Fig 15. Schematic of a radial junction rod cell. This shows the dimensional parameters of the p and n regions and energy band diagram through the radius of the device [93]

The minority carrier diffusion in the quasineutral regions was calculated using transport equations and dependant on the excess minority concentration (doping density), the minority carrier diffusion length, material absorption co-efficient, photon flux and minority carrier diffusion co-efficient. The depletion region current was calculated based on the assumption that all absorbed light produced collected carriers, whilst the depletion region width was calculated using Poisson's equation. The recombination current density was approximated

on the assumption that the voltage potential within the depletion region was linearly dependant on the rod radius.

Short circuit current density (J_{sc}) for the planar devices was found to be closely related to minority carrier diffusion length whilst that for the rod devices was broadly independent as expected from theory. This confirms the principle that rod devices may be fabricated from a lower quality material with greater defect density than planar devices for equivalent or superior J_{sc} performance. Open circuit voltage (V_{oc}) for the planar device was broadly constant for all values of cell thickness and carrier diffusion length. In the case of the pillar cell, however, it decreased with wire length for the pillar devices due to the increasing junction area. Of greater interest was the effect of trap densities on V_{oc} particularly for rod devices. The V_{oc} dropped from 0.58 V to near 0 V if the trap density in the bulk material was increased but only fell to 0.38 V if the trap density in the depletion region was retained at a lower level. The planar device suffered less detrimental effect with a fall from 0.59 V to 0.24 V for a constant bulk trap density and to 0.49 V if the depletion region trap density was maintained at a lower level.

Fill factor (FF) was also briefly considered and followed a similar trend to V_{oc} whereby a low trap density in the depletion region resulted in a fill factor >80% almost irrespective of that found in the quasineutral region. A fall in carrier lifetime in the depletion region, however, impacted sharply on the FF for the pillar devices and to a lesser extent that of the planar devices.

It can be inferred, therefore, that radial p-n junction devices are capable of good performance with high defect concentration material provided the trap density in the depletion region itself is maintained at low level. This is in agreement with the observations of Catchpole et al [108] when comparing planar and rod devices.

The optimal rod dimensions were inferred to be achieved when the rod radius was equivalent to the minority carrier diffusion distance and a length equivalent to the optical thickness, providing that the key requirement of a low trap density in the depletion region is met. For the case of higher trap densities, thinner rod devices are superior. Regarding the emitter, it was noted that the ideal case is high doping in both the p and n-type regions (without excessively compromising carrier lifetime, particularly in the core region) as whilst high doping reduces mobility it improves V_{oc} . This is particularly relevant for rod devices where the V_{oc} is generally lower due to increased junction area.

Foldyna et al [109] simulated square and hexagonal arrays of silicon nanowires by 3D rigorous coupled wave analysis (RCWA). They selected dimensional values for diameter of

100-700 nm, lengths in the range 1-10 μm with wire pitches of 0.4, 0.6, 0.8 and 1 μm . They noted, in agreement with [101] that there is little difference in performance between square and hexagonal wire arrays as the confinement properties of the structures are largely independent of structure organisation. Also of interest is their note that maximal performance for hexagonal arrays is shifted towards larger wire spacing, potentially straying into the low micron range which is an area of interest for this project. It was suggested that 5 μm is the optimal length for J_{sc} when considering the trade-off between enhanced performance and increased fabrication difficulty with a value of 31 mA/cm² predicted at this dimension.

In the work by Gharghi [110], rods on the micron scale were assessed using a drift-diffusion transport model, albeit with the prime goal of investigating the use of upgraded metallurgical grade silicon (UMG). The model evaluates the probability of a generated carrier reaching the junction based on the distance from the space charge region (SCR) and from this a value for internal quantum efficiency (IQE) can be determined. The model considers the generation under normal incidence of illumination which due to the rotational symmetry of the pillar permits the pillar to be modelled as a two dimensional structure. Furthermore, to focus on the radial geometry, the effect of a planar junction at the base or interface at the top of the pillars is ignored.

As has been observed in the previous model, the greatest collection probability is observed for a pillar where the radius is equal to the minority carrier diffusion length. A 90% collection probability is observed for this configuration and it is noted that there is no significant improvement achieved by reducing the radius below this value. Comparing the collection probability between a radial junction and planar junction, it is shown that for carriers generated at a given distance from the junction the collection probability is always higher in a pillar structure. This is related to the increasing ratio of collection area (junction) to generation volume (pillar bulk) with decreasing pillar diameter (and therefore increasing pillar concentration). It is acknowledged, however, that as noted previously, increased surface area can result in increased saturation current and reduced cell voltage.

Regarding the emitter formation, a shallow emitter is considered to be optimal which is in agreement with the aforementioned and other work [111][112] but, as has been noted, shallow emitters must be very highly doped to achieve the necessary sheet resistance [113]. For this approach to be effective, very high levels of passivation must be achieved, as noted by M. Zanuccoli et al in their modelling work [114] where increasing surface recombination values (SRV) from a poorly passivated highly doped emitter resulted in rising efficiency losses.

A practical example was considered which consisted of a 20 μm height rod with a 300 nm emitter and doping levels of 1×10^{17} and 1×10^{19} atoms/cm³ in the base and emitter respectively with good passivation for an SRV of 1×10^3 cm/s. The result is an optimum pillar radius of 3.2 μm with regard to photocurrent generation which is similar to the estimated minority carrier diffusion length in the upgraded metallurgical grade silicon. This lends credence to the argument that larger structures can exhibit superior electronic performance when compared to their optically advantageous nano-scale counterparts. It is relevant to note the suggestion that the advantage of nano-pillars is reduced as the radius shrinks substantially below the minority carrier diffusion length, indicating that reducing their radius to achieve peak absorption may simply make fabricating an effective electron device more difficult [115] for little overall benefit.

2.14. Fabricated Device Performance

An early practical implementation of a solar cell with decoupled optical absorption and carrier collection was described as a vertical junction solar cell. Developed by Lindmayer and Wrigley [116], grooves in the region of 7 μm wide at 50 μm spacing and depths of 150 μm were fabricated by oxide masking, photolithography and wet alkaline etching. These devices achieved 13 % efficiency and 78% fill factor under AM0 conditions (devices were developed for space application hence the non AM1.5(G) measurements).

Further development by Wholgemuth and Scheinine [117], resulted in devices with grooves of a similar width and spacing but depths reduced to 25 μm or 75 μm . Devices demonstrated efficiencies in excess of 15% and fill factors approaching 80%, comparable to equivalent planar devices but with a reduced V_{oc} value (< 600 mV) due to the increased surface area. Whilst these devices were designed for space applications with enhanced radiation resistance, this was achieved in the same way as the radial junction geometry by shortening the minority carrier diffusion length.

Tsakalakos et al [118] demonstrated a silicon nanowire device with wires fabricated by the vapour-liquid-solid (VLS) growth method and a conformal amorphous silicon (a-Si:H) emitter. The wires were on the order of 100 nm diameter and 16 μm in length. The authors noted the advantage of using a-Si:H as the emitter as it possesses good passivation properties and as has been previously discussed this is crucial for good device operation. The arrays demonstrated a real world reduction in reflection of one to two orders of magnitude over a planar device which provides good validation of the previously reviewed modelling work. Electronic performance was relatively poor with low V_{oc} of 280 mV and conversion efficiency of ≈0.1 % but with clearly rectifying performance despite the fill factor only reaching 28%.

The authors cited the discrepancy between wire diameter relative to the minority carrier diffusion length and lack of optimisation of the doping levels of the core and shell of the devices as performance limiting factors. This is in agreement with the work by Kayes et al [119] which suggests that these factors are crucial to obtaining best efficiency. Also of note was the method of wire growth utilising gold (Au) as a catalyst metal which is known to be detrimental to lifetime in silicon [120], indicating the challenges of fabricating structures by the VLS method.

Garnett and Yang [121] fabricated silicon nanowires by a solution-phase etching method which utilised silver nitrate and hydrofluoric acid to etch arrays of vertical aligned structures. These were on the order of 100 nm diameter and 18 μm length. Amorphous silicon was utilised as the emitter with a doping concentration on the order of 1.7×10^{19} atoms/cm³, compared to the base wafer doping of 1×10^{16} atoms/cm³. Similar V_{oc} values to those observed by Tsakalakos were measured, demonstrated by the high dark current observed, and were related to the high recombination resulting from the large surface area. The authors noted that similar wires but with a deep lying, non-radial junction demonstrated substantially better efficiencies (up to $\approx 9.5\%$ for wires etched into single crystal wafer) [122] reinforcing the idea that recombination losses are a major limiting factor for structured device performance, particularly regarding V_{oc} .

Wang et al [123] reported fabrication of periodic, uniform, vertically arrayed nanowires. This was achieved by patterning of a gold (Au) catalyst layer by nanosphere lithography to achieve a film with regularly spaced, circular openings. By subjecting this catalyst layers to an electrochemical etch process which preferentially etches under an Au film, arrays of 670 nm diameter, 0.33 μm to 5.33 μm length nanowires were prepared. As previously observed for structures of this scale, low reflectance (<15%) over a wide spectral range (250 nm – 1200 nm) was achieved with improving performance with increasing nanowire length. Emitter formation was achieved by application of a spin on dopant solution followed by a drive in process. Emitter concentration was found by secondary ion mass spectroscopy to be in the region of 8×10^{18} atoms/cm³, compared to a base wafer concentration of 5×10^{18} atoms/cm³. Dark I-V analysis demonstrated an ideality factor (4.4), substantially lower than that found by Wang et al and resulting in a superior V_{oc} of 0.45 V and a fill factor of 53%. The enhancement is attributed to the improved quality of the junction prepared by the diffused doping process with uniformity of diffusion into the nanowires demonstrated by SIMS analysis.

Garnett and Yang [124] developed their process further from [121] to produce nanowires with superior surface finish and greater control over diameter and density. A regular array of

silica beads was applied to the wafer surface acting as a mask for a deep reactive ion etching (DRIE) process. The result after different etch times were periodic, uniform array of nanowires with average dimensions of 390 nm width and 5 μm or 20 μm lengths. I-V analysis yielded V_{oc} values of ≈ 520 mV for the shorter wires and ≈ 560 mV for the longer wires with fill factor values in the region of 57% for both lengths, significantly higher than other results prior to this point. The authors noted that whilst the 8 μm length wires exhibited an efficiency of 4.83%, which exceeded that of an equivalent thickness planar device, the 20 μm equivalent planar device exceeded the 5.30% efficiency demonstrated by the longer pillars. It was posited that for thinner absorbers, light trapping is most crucial, whilst for thicker layers that are already reasonable absorbers, electronic properties such as recombination dominate the efficiency losses.

This was confirmed by Li et al [125] in their work on variable length nanowires. Their wires were prepared on a silicon wafer substrate which was amply thick to absorb all non-reflected incident light; therefore electronic effects should dominate performance. They noted that despite the wires showing excellent anti-reflection properties, even the shortest wires of 1 μm showed a 1.5% absolute efficiency loss to 11.1% compared to the planar control at 12.6% with the longest wires of 6 μm falling to 2% efficiency.

Yoon et al [126] adopted a similar approach to Garnett and Yang, forming wires by DRIE but in this case with an SiO_2 mask, patterned by optical lithography [127]. Wires were on average 25 μm in height but more notably had a diameter of approximately 7.5 μm and are more properly referred to as micro-pillars due to their scale. To assess the effect of using silicon with short carrier lifetimes, they selected wafers with high doping concentrations; 5×10^{18} atoms/cm³ and 7×10^{19} atoms/cm³. They formed emitters by gas phase diffusion using phosphorus oxychloride (POCl_3) with junction depths on the order of 0.2-0.3 μm . As expected, the pillars formed on the most highly doped wafer substrates performed less efficiently (3.7%) than those on the more lightly doped substrate (8.7%). However, in both cases, the pillar devices still outperformed their planar counterparts highlighting the resilience of the radial junction structure to short minority carrier diffusion lengths. Additionally, the high values for V_{oc} of 560 mV and fill factor of 78% demonstrate that excellent electronic properties can be more straightforwardly achieved on micron scale structures.

Gharghi et al [128] built on their theoretical work [110] and fabricated micron scale pillar arrays by photolithography and DRIE in UMG silicon with short carrier lifetimes. Their devices contained pillar features with widths in the range 1.5 μm to 50 μm , height of 22 μm and a D/P ratio of 0.73 falling well within the ideal dimension value discussed in the

modelling section of this work. In contrast to Yoon et al they fabricated their emitter using amorphous silicon with a thin intrinsic silicon layer between it and the surface of the pillars. This is based on the HIT structure [76] as developed by Sanyo (now Panasonic) which is demonstrated to exhibit the low saturation current crucial to effect operation of a structured device. It was noted post fabrication there was significant surface damage and contamination [129] resulting from the etch process and devices with emitter layers fabricated directly atop this surface produced shunted devices with low open circuit voltages (200 mV). Multiple oxidation [130] and buffered hydrofluoric acid etches [131] resulted in significant removal of contaminants and reduction in side wall roughness which was found to be critical for achieving the very high surface passivation achievable by using a:Si. Notably, Yoon et al made similar observations for their work with diffused emitters indicating that surface finish of devices and its effect on recombination is important irrespective of emitter formation method. Best performance was found for pillars of 15 µm diameter with 12.2% efficiency, V_{oc} of 591 mV and FF of 66%. The front contact utilised was aluminium doped zinc oxide (AZO) which, to protect the amorphous silicon emitter [132], had to be deposited at low temperature increasing its resistivity and reducing performance [133]. This validates AZO as a potential front contacting method for micron scale pillar device and, provided high temperature deposition is compatible with processing techniques utilised in this work, AZO with lower resistivity and accordingly reduced performance losses should be attainable.

Kim et al [134] adopted a similar approach to [126] for fabrication and doping, via DRIE and diffusion doping but utilised high quality single crystal wafers with resistivity in the range 1-10 Ω/cm^2 giving high minority carrier diffusion lengths. Structures of 2 µm diameter, spaced at 7 µm and 4 µm and of 5 µm diameter, spaced at 7 µm and 10 µm were fabricated. Post diffusion the devices were passivated with plasma enhanced chemical vapour deposited SiN_x to minimise recombination [135]. All devices exhibited superior efficiencies (best at 16.2%) to the planar device at 14.3% along with superior J_{sc} . More notably all devices exhibited superior V_{oc} to the planar devices which is likely attributable to the more modest increase in surface area achieved by these wide and relatively short pillars as compared to that of vast quantities of nano scale width and micron scale length nanowires. It also suggests that according to the modelling in [93] that defect levels in the space charge region must be low indicating that a high quality junction has been achieved, likely due to the use of a diffusion doping process in high quality substrate material.

Mallorqui et al [136] investigated the effect of varying the substrate wafer doping level on performance of micro-wire devices and the importance of scaling the doping densities depending on wire diameter to ensure the depletion region dimensions are appropriate. Pillars of diameters 1.86 µm, 2.4 µm and 3.1 µm and length 45 µm were fabricated with

spacings of 7, 8 and 10 μm respectively. The substrates used had resistivity's of 0.1-0.5, 1-5 and 1-10 Ω/cm^2 and the device's emitters were formed by POCl_3 diffusion [137]. Examining the values for J_{sc} and efficiency reveals a requirement for increasing base wafer doping with shrinking pillar diameters. This is in agreement with theory [138] as increasing doping levels will result in a shrinking depletion region required to maintain an active carrier region in the core of the rods. However, lower doping levels produce superior electronic performance in general and therefore larger diameter pillars which can tolerate the lower doping levels without becoming depleted demonstrate superior performance to the smallest diameter pillars. Notably, with the exception of the smallest diameter pillars, when optimally doped all devices exhibit superior performance to the planar devices. Also of relevance is the tolerance of these micron scale devices to changes in V_{oc} with only one sample showing more than a 20 mV voltage drop compared to the best planar device. This reinforces the argument for micron scale devices being more electronically resilient than nano scale devices despite their less effective anti-reflection properties. It was also noted that emitters diffused at 850 °C, for a junction depth of 270 nm, exhibited higher EQE performance than those at 900 °C which have an emitter depth of 635 nm. Due to the high doping concentration in the emitter, this is a region in which photogenerated carriers are inefficiently collected [139] and therefore as the emitter widens, efficiency falls.

In a series of papers Elbersen et al [140][141][142] investigated a variety of methods for fabricating emitters in nano and micro scale pillar arrays. They observed that a key issue with emitter formation in structured devices is that the junction formation technique used is often monitored on a planar control. This approach does not provide any verification of the doping techniques ability to form a homogeneous emitter on a structured device, especially when considering pillars with high aspect ratio or arrays with high packing fractions.

To investigate the performance of various doping methods, arrays of 4 μm diameter, 1-60 μm height pillars at 2 μm spacing were fabricated as test structures in p-type and n-type wafers. The techniques examined were solid state diffusion (SSD)[143], low pressure chemical vapour deposition (LPCVD)[144], atmospheric pressure chemical vapour deposition (APCVD)[145] and plasma enhanced chemical vapour deposition (PECVD)[146]. APCVD was not available as a potential doping technique for this project and PECVD was noted to be ineffectual at depositing conformal layers on vertical structures, which was in agreement with experimentation carried out at LSBU. As such neither of these techniques is considered further in this review. Both SSD and LPCVD were demonstrated to produce homogeneous emitter layers on the structured devices by focused ion beam (FIB) milling [147] of pillar structures and staining to highlight the junction position. All arrays, provided they were not excessively doped, demonstrated efficiency enhancement over their planar

counterparts and notably improvements were more pronounced for n-type emitters diffused into p-type wafers. However, control of the junction position was shown to be critical as intentionally over diffused devices demonstrated severe J_{sc} losses resulting in performance that was significantly worse than the planar devices.

The effect of pillar length was investigated with performance found to rise steadily until a length of 40 μm was reached before falling due to a decline in J_{sc} . This is in contrast to the peak predicted performance of Voight et al [148] who concluded that the best result would be achieved for a 96 μm pillar with 2 μm diameter. Clearly this highlights that there are many factors which affect real world devices which are challenging to include in a modelled scenario. Notably they found a rising trend of V_{oc} with pillar height (and by extension junction area) which is contrary to theory [149]. It should be pointed out, however, that the measured values are significantly lower than conventional silicon devices (< 500 mV). The authors theorised that this rise in V_{oc} was related to the increasing (but well passivated by SiN) junction area improving the junction potential. Considering the large scale of the features (tens of microns vs nanometres) this seems a plausible explanation and adds confidence to the argument that large scale structures have definite electronic advantages over nano scale devices.

Finally, the effect of junction depth was investigated. Best device performance was found for a junction depth of 790 μm with shallower and deeper junctions demonstrating inferior performance. The junctions shallower than 790 μm showed reduced J_{sc} but also a poor fill factor, suggesting that the problem was related additionally to an inadequate level of doping causing poor charge separation rather than simply the junction depth. This was backed up by the data for the deeper high temperature diffusions, which showed reduced J_{sc} but good fill factor. It is proposed that if a shallow junction that retains high levels of doping can be achieved, this should provide superior performance, which is in agreement with literature [150].

2.15. Contacting

There are two contacting technologies utilised in this project, metal and transparent conductive oxides (TCO). More technical details will be addressed in the experimental section; however, a brief discussion of their principles and properties is appropriate here.

Contacting of semiconductor devices is a field that has undergone substantial study in its own right due to the potential for device affecting performance gains or losses. Contacting techniques varying significantly depending on material and device configuration and will be broken down into metal contacts and transparent conductive oxides (TCO).

2.15.1. Metal Contacts

There are three principle types of contact between a metal and a semiconductor; ohmic, tunnelling and Schottky.

According to the Schottky-Mott rule, an ohmic contact is formed between a metal and a semiconductor when the Schottky barrier height ($e\Phi_B$) is low[151]. In this condition, electrons are free to flow in and out of the material with minimal resistance in the circuit.

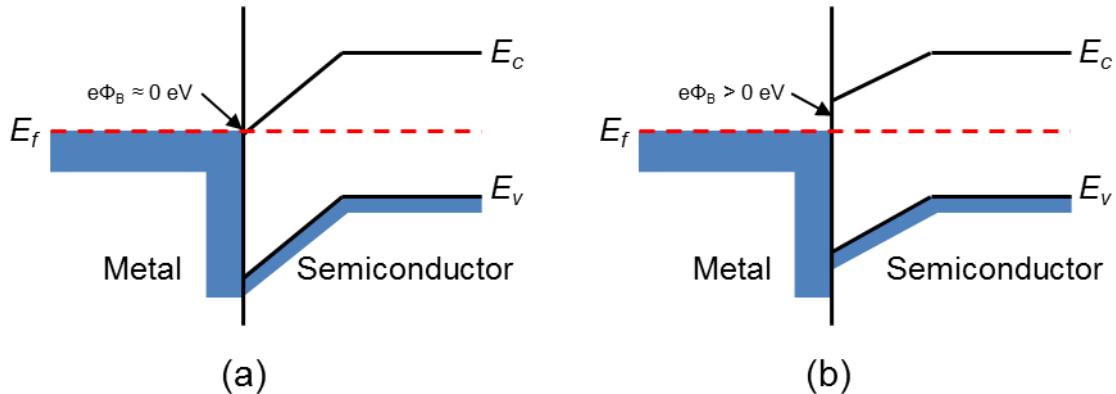


Fig 16. Band diagram for an ideal ohmic contact. **(a)** Demonstrating the band bending resulting in the semiconductor conduction band meeting the metal fermi level and leading to a near zero Schottky Barrier Height. **(b)** Showing the effect of Fermi pinning and the resulting Schottky barrier height, which inhibits contact performance.

The Schottky-Mott rule relies on the theory that the semiconductor's bands will experience band bending when brought into contact with a metal, whereby the semiconductor's work function matches that of the metal (Fig 16). The work function is defined as the minimum energy required to liberate an electron from a solid to a point in a vacuum directly adjacent to the material [152]. In reality, a phenomenon described as Fermi level pinning results in unpredictable final positioning of the semiconductor's bands due to energy states at the semiconductor surface [153]. These states can effectively absorb much of the charge donated by the metal surface and prevent the predicted band bending. As a result, much of the understanding about metal choices for semiconductor contacts has developed from experimentation rather than theory.

An alternative approach to obtaining an ohmic contact, which does not rely on achieving a near zero Schottky barrier height, is to form a tunnel junction [154]. This type of contact possesses a positive Schottky barrier height, but the doping in the semiconductor is raised to such a level that the depletion region between the metal and semiconductor is suitably thin that electrons are able to "tunnel" across the interface (Fig 17). It is not possible to explain

the process of tunnelling using classical physics, where an electron presented with the positive barrier height would have a zero probability of passing. However, due to the very small distances involved, quantum mechanics suggests the possibility of electrons passing directly through the barrier based on the uncertainty principle.

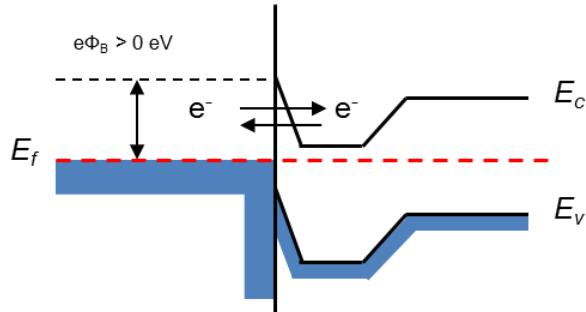


Fig 17. Band diagram for a tunnel junction contact. Here the doping level in the semiconductor is raised to a level high enough that the depletion region is adequately narrow so as to permit quantum tunnelling.

A Schottky barrier contact is one where the Schottky barrier height ($e\Phi_B$) is positive and a depletion region exists at the interface (Fig 18). At this point the flow of electrons across the junction is controlled by thermionic emission, much like a semiconductor junction. Therefore at low bias values the contact interface is highly resistive but as the bias is increased many thermally excited electrons are able to pass over the junction with current flow rising rapidly with bias.

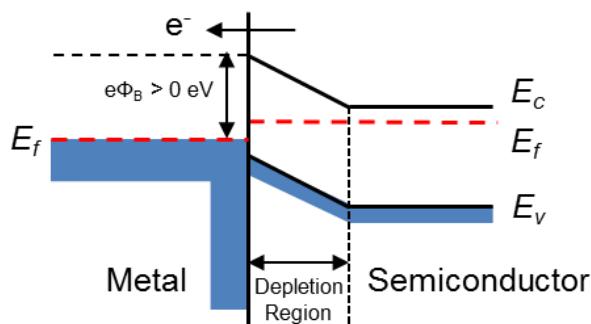


Fig 18. Band diagram for a Schottky contact. Here a depletion region exists between the metal and the semiconductor and the flow of electrons is subject to adequate bias being available to promote electrons to the conduction band and pass over the barrier between the two materials.

It is of course relevant that, as a result of the depletion region, the Schottky contact is rectifying and thus its use as a contact is dependent on device configuration.

The contact metals typical used in silicon PV technology to make low resistance contacts have been highlighted in section 2.10 above.

2.15.2. Transparent Conductive Oxide (TCO)

A complementary technology to metal contacts which has grown out of the development of the semiconductor industry is that of the Transparent Conductive Oxide (TCO). This has been particularly critical in the advances in LCD, TFT, OLED and touch screen device design. However, TCO technology also offers the possibility of useful enhancement to the photovoltaic industry by permitting carrier collection from the entire front surface of a cell whilst reducing or eliminating contact shading [155]. Consequently, TCO contacts are widely used in all thin film PV technologies [156]. They are also a crucial technology for the successful fabrication of tandem solar devices as they provide the electronic interface between the different device layers [157]. Notably, despite the common usage in thin film devices, they have yet to see significant use on crystalline silicon. This is arguably due to the relatively limited potential performance gain versus the increased cost of the TCO material and greater manufacturing complexity.

In principle, a TCO is degenerately doped semiconductor, which due to the very high level of dopant incorporation behaves like a metal. However, TCO's also generally have large band gap energies; resulting in them transmitting much of the optical spectrum, hence their moniker. Important attributes for TCO's are consistently high optical transmission across the visible spectrum and a low sheet resistance. The properties of some common TCO materials are tabulated in Table 1.

Name	Typical Band Gap	Sheet Resistance	%T	Limitations
Aluminium doped Zinc Oxide (AZO)	3.4 eV [158]	7 Ω/□ [159]	>80 % [159]	-Difficult to pattern accurately -Lower transmission
Indium doped Tin Oxide (ITO)	3.7 eV [160]	7 Ω/□ [160]	>85 % [160]	-Rarity of indium -Affected by annealing in air
Fluorine doped Tin Oxide (FTO)	3.8 eV [161]	12 Ω/□ [162]	>83 % [162]	-Difficult to achieve best sheet resistance by sputtering
Cadmium Oxide (CdO)	2.2 eV [163]	16 Ω/□ [164]	>85 % [165]	-Unstable (hygroscopic)

Table 1: Comparison of the properties of various common TCOs

The earliest reported TCO was cadmium oxide (CdO) in 1907 and was prepared by the post evaporation oxidation of a thin film of pure cadmium [166]. Whilst doping of CdO with elements such as tin and indium has demonstrated improvements above those parameters listed in Table 1, its hygroscopic properties make it a challenging material to work with.

The most common TCO in use today is tin doped indium oxide or ITO [167]. It is conveniently deposited by sputtering and can be straightforwardly patterned and etched. Despite this dominant position and advantages, the abundance of indium is in question and could potentially limit the maximum future production rate of ITO. Additionally, ITO is affected by temperature which places restrictions on its use where thermal processing steps are required [168].

An alternative to ITO is fluorine doped tin oxide (FTO) which dispenses with the rare indium component. It's possesses slightly poorer optical and electronic properties than ITO and notably it is challenging to achieve its highest performing parameters by sputtering which is a commonly preferred approach in industry [169]. However, unlike both ITO and AZO, FTO demonstrates excellent resistance to thermal annealing which gives it a significant advantage for application where high temperature processing of films or use in high temperature environments is required.

The final TCO to be mentioned is that of aluminium doped zinc oxide (AZO). It can be conveniently deposited by sputtering [170][171][172], contains no rare materials and whilst demonstrating slight poorer optical and electronic properties than ITO [173] it demonstrates superior electronic properties to FTO. A limitation for AZO is its inferior patterning properties, although this is generally a greater concern for display applications. Additionally, whilst AZO demonstrates weaker chemical resistance compared to FTO, intentionally chemically textured AZO has demonstrated effective light scattering and trapping properties [174].

Due to LSBU possessing the ability to deposit AZO by magnetron sputtering, it was decided to carry out a two stage investigation into films prepared by this method. The first was to establish the properties of the AZO films in isolation by depositing them on glass, whilst the second was the effect of applying optimal films to complete solar devices. The results of this investigation are covered in detail in the experimental portion of this work with deposition parameters examined in chapter 4, anti-reflective properties discussed in chapter 5 and electronic performance examined in chapter 6.

2.16. Conclusions

- This chapter has reviewed the relevant background, literature and current state of the art in relation to the field in which this project is to be undertaken. The existing first generation (silicon) and second generation thin film solar technologies have been reviewed to place the micro-rod solar cell concept into context. Silicon can gain a significant advantage over existing thin film technologies if currently achievable efficiencies can be retained whilst material usage is reduced.
- A survey of the optical performance of wire and rod based solar cells shows that features on the order of tens or hundreds of nanometres exhibit excellent anti-reflective properties and optical absorption with overall thicknesses substantially less than that of current silicon wafer based devices. However, these features are typically formed by self-organising techniques which limit the level of precise refinement which can be applied to tune the optical performance. Larger features on the micro-scale demonstrate less favourable optical properties; however, features at the transition point between the nano and micro scale still demonstrated useful enhancements. A common feature of all the work was the idea of an optimum diameter/periodicity (D/P) ratio of ≈ 0.7 .
- A review of the electronic performance modelling of rod structures showed that optimal performance of radial junction solar cells was generally contingent on shallow, highly doped emitters with the resulting requirement of excellent passivation to mitigate recombination losses. This is a challenging list of requirements with elements which are often contrary to each other. Better performance was generally observed for larger diameter structures. This agreed with the idea that large surface area emitters (i.e. with smaller and more numerous features) would suffer greater dark saturation current and losses to V_{oc} and performance in general.
- The investigated experimental device literature yielded generally good agreement with that suggested by modelling. Fabrication of devices on smaller diameter structures generally yielded poor V_{oc} and efficiency values, particularly when the features were wet etched using self-organising processes. Larger scale features on the micro scale typically yielded better performance. This was especially true when the features were fabricated by an organised process such as lithography and DRIE due to superior surface finish. This suggested that whilst demonstrating inferior optical properties, larger structured samples may be able to offset this loss by being more straightforward to fabricate effective electronic devices from.

- The theory of device contacting has been briefly reviewed and discussed conventional metal contacting as well as transparent conductive oxide (TCO) technology.

Chapter 3. Experimental Techniques

This chapter describes the experimental and characterisation equipment and techniques that formed an integral part of this body of work. First the various processes used for device fabrication including diffusion and contact formation and secondly the techniques used to characterise processed samples and complete devices.

As impurity doping is a major feature in this project, predominantly for emitter formation but also for certain types of contact formation, the process will be explored in detail. This will include diffusion theory, the various means by which diffusion doping can be achieved and the challenges involved in producing emitters suitable for micron scale features.

Conventional solar emitter formation will be introduced along with the technique ultimately utilised in this project. The processes necessary for effective p-n junction operation post diffusion will also be discussed, including edge isolation and passivation.

Diffused emitter devices require processing into a complete cell for performance characterisation to take place which necessitates deposition of metal layers for contact formation. This was carried out using a combination of thermal evaporation and RF magnetron sputtering followed by thermal annealing to ensure the ohmicity of deposited contacts. Thermal annealing was achieved by tube furnace or rapid thermal processing. The aforementioned techniques will be discussed along with their ancillary requirements such as film thickness monitoring and temperature control.

Sample characterisation fell into three categories; physical, optical and electronic sample properties. Physical properties included feature dimensions and appearance and thin film characterisation. The former was assessed by scanning electron microscopy (SEM) which permitted close analysis of the features as a whole as well as ancillary detail such as damage or the conformity of applied coatings. Thickness of deposited layers was carried out either by stylus profilometry or ellipsometry for very thin layers where mechanical measurements techniques approached their resolution limits.

Optical properties, predominantly the level of reflection of structured devices but also the transmission of transmitting conductive oxides (TCO) on glass, were assessed by spectrophotometry.

The electronic properties of devices were assessed both during device fabrication and after complete solar cells were prepared. Doping concentration was assessed by four point probe whilst carrier concentration and mobility for both diffused emitters and deposited TCO layers was measured using the Hall Effect technique. Suns-Voc was used during device

development to permit the monitoring of incomplete devices and assess the performance of emitters.

Completed solar cells were characterised by I-V analysis under dark and one sun illumination using a solar simulator. The spectral response of devices was also characterised which permitted their quantum efficiency to be calculated.

3.1. Impurity Diffusion in Semiconductors

The doping of semiconductor materials with impurities to change their properties is a well-understood and heavily documented process. It serves two purposes in this project, the first being incorporation of impurities for emitter formation and the second being for ohmic contact formation in particular circumstances. The choice of impurities utilised is dependent on the semiconductor material whose properties are being manipulated.

3.1.1. Diffusion Mechanisms

The key variables involved when considering diffusion doping are the dopant concentration gradient, the diffusivity on the impurity and the temperature under which the diffusion takes place. The movement of impurity atoms within the semiconductor lattice is a nominally random process but occurs by one of a number of mechanisms [175] of which the principle methods are shown in Fig 19.

Interstitial diffusion is the movement of impurity atoms between vacant interstitial sites (gaps between lattice atoms). This type of diffusion requires that the diffusion motion occur from one interstitial site to another adjacent interstitial site. This process is relatively rapid as there is a large number of this type of vacancy in a semiconductor. This is particularly true when considering silicon due to its loosely packed crystal structure [176].

Substitutional diffusion is the movement of impurity atoms between one lattice site and the next where the impurity substitutes for the host atom [177]. This type of diffusion requires lattice vacancies and indeed ones that are adjacent to permit the impurity atom to move from site to site. These vacancies are present in even the purest single crystal semiconductors, however, due to the smaller number of lattice vacancies relative to interstitial vacancies, substitutional diffusion occurs at a slower rate than interstitial diffusion.

A variation of the interstitial diffusion process is interstitial-substitutional diffusion by the kick-out mechanism [178]. Here, a high energy interstitially diffusing atom can transition to a substitutional site by displacing an existing atom, resulting in the production of a self-

interstitial. The production of self-interstitial atoms is necessary for the interstitialcy diffusion mechanism to be considered.

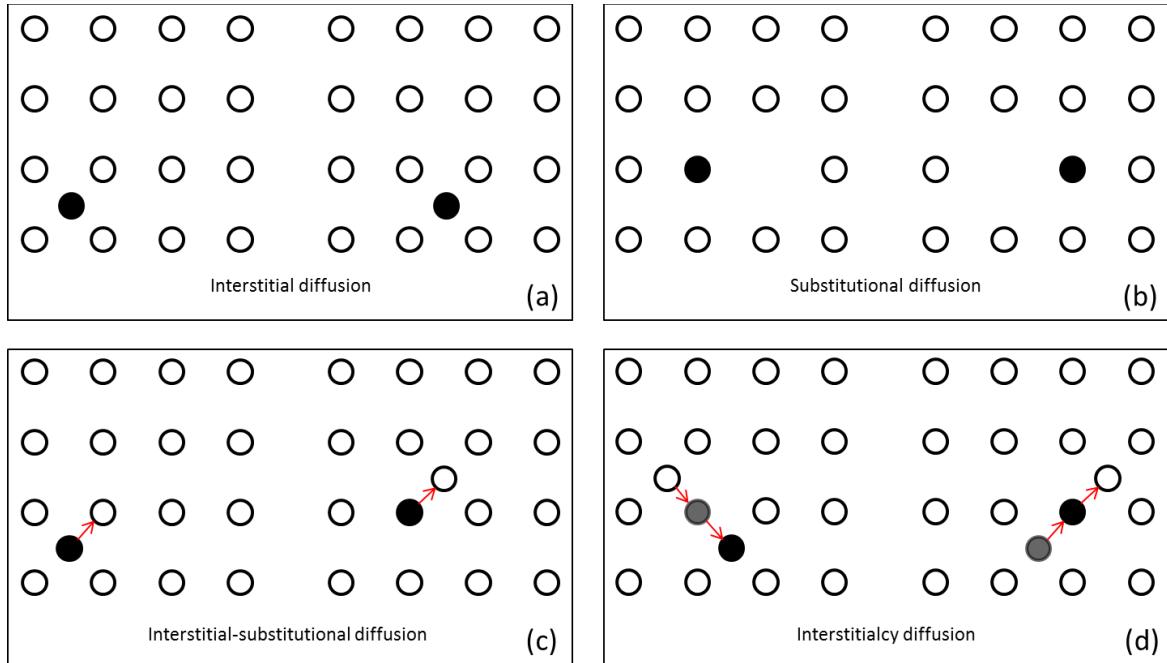


Fig 19. Impurity diffusion mechanisms in silicon. **(a)** Interstitial diffusion takes place when impurity atoms move between the interstitial sites which lie between lattice atoms. **(b)** Substitutional diffusion takes place when impurity atoms move between adjacent, vacant lattice sites where the impurity atom substitutes for a host atom. **(c)** Interstitial-substitutional diffusion occurs when an interstitially diffusing atom, with sufficient energy, displaces a host atom by the kick-out mechanism and creates what is referred to as a self-interstitial host atom. **(d)** Interstitialcy diffusion occurs when a self-interstitial host atom, which has been displaced by a substitutional impurity atom, forces another impurity atom out of a lattice site and places it back into the interstitial position. Here it diffuses to another site and undertakes further interstitial-substitutional type diffusion.

Interstitialcy diffusion is a variation of the substitutional diffusion process. In this process, self-interstitial host atoms (native lattice atoms which have been displaced) can force substitutional impurity atoms into interstitial positions. These can now diffuse to nearby substitutional sites and via the kick-out mechanism replace a host atom producing a new self-interstitial host atom. Due to the combination of interstitial and substitutional diffusion mechanisms, this process occurs at a higher rate than substitutional diffusion alone. Furthermore, in reality, all substitutional diffusion occurs in some part by this mechanism and indeed the majority of boron and phosphorus diffusion in silicon is in fact by this method [179].

A final diffusion mechanism worth mentioning is that which occurs along lattice dislocations and grain boundaries [180]. Where diffusing impurity atoms meet a grain boundary or dislocation, they diffuse at an anisotropic rate parallel to the dislocation core or boundary edge, potentially several times faster than by the conventional diffusion mechanisms. This is often problematic as it can lead to the formation of highly doped regions, potentially resulting in shunting paths through emitter layers.

The movement of impurity atoms in a semiconductor is temperature dependant and random in nature. However, in the presence of a concentration gradient, the diffusion process is directed.

The following section discusses the various means by which a concentration gradient may be achieved and the various calculations that permit the resultant dopant profile and concentrations may be approximated.

3.1.2. Diffusion Calculations

Using a variation of Fick's second law [181] it is possible to approximate the depth of dopant diffusion.

In the simplest form Fick's second law states:

$$\frac{\partial N(x,t)}{\partial t} = D \frac{\partial^2 N(x,t)}{\partial x^2} \quad (3.1)$$

Where $N(x, t)$ is the concentration of diffusing substances (atoms/cm²) at point x and time t and D is the diffusion coefficient of the material which is strongly dependent on temperature (cm²/s).

There are two solutions by which the partial differential equation may be solved. The first assumes the dopant source at the surface of the material to be doped (N_s) is constant and inexhaustible. The second assumes an exhaustible dopant supply at the surface with a given concentration.

3.1.2.1. Constant Source Diffusion

In the first instance, where the dopant source is inexhaustible, the distribution is described by the complementary error function (erfc):

$$erfc(x) = 1 - \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \quad (3.2)$$

The boundary conditions for this solution are:

Surface concentration (N_s) is constant where $0 < t < \infty$, diffusion depth ($N(x)$) = 0 where $t = 0$ and $0 < x < \infty$.

Therefore equation 3.2 becomes:

$$\operatorname{erfc}(x) = 1 - \frac{2}{\sqrt{\pi}} \int_0^{\frac{x}{2\sqrt{Dt}}} e^{-t^2} dt \quad (3.3)$$

This can be simplified to an equation based around the complementary error function (erfc):

$$N(x, t) = N_s \operatorname{erfc} \left\{ \frac{x}{2\sqrt{Dt}} \right\} \quad (3.4)$$

The erfc function (also referred to as the inverse Gaussian error function) is commonly used in probability theory as a means to represent the probability that a given parameter falls outside a specified range. In diffusion theory it conveniently accounts for the distribution probability of a diffusing dopant species in a semiconductor.

Figure 20 shows the plotted relationship between the ratio of concentrations (N_{xt}/N_s) and the argument $x/(Dt)^{0.5}$. The ratio (N_{xt}/N_s) describes the ratio between the background doping of the substrate wafer and that of the doping concentration at its surface. The plot permits convenient solving of equation 3.4 by reading off the solution to $x/(Dt)^{0.5}$ based on the N_{xt}/N_s ratio rather than necessarily solving the erfc function for a given set of variables.

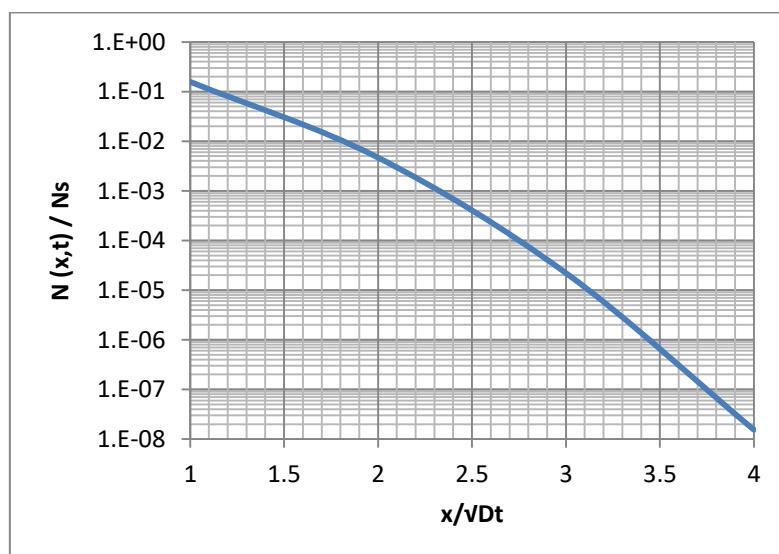


Fig 20. Concentration distribution according to the erfc distribution given in equation 3.4

It is generally assumed that the doping concentration at the wafer surface is very large and therefore the surface concentration N_s is set as the solid solubility of the diffusion impurity at the temperature for which diffusion is taking place.

A diffusion of this type is utilised when a high surface concentration is necessary and can be adjusted by modifying the temperature at which the diffusion is undertaken. The caveat to this statement is that the time taken to achieve a deep emitter with low surface concentration (necessitating a low diffusion temperature) would be prohibitively long for practical purposes.

This type of diffusion is typically achieved in a diffusion furnace through which an impurity containing gas is flowed or a solid source of the impurity material is placed. This ensures a constant supply of dopant throughout the diffusion process.

3.1.2.2. Limited Source Diffusion

In the second instance, a finite amount of impurity is deposited on the surface of the wafer and diffusion occurs from this limited source. The resulting distribution is described by the gaussian distribution:

$$N(x, t) = \frac{Q_0}{\sqrt{\pi D t}} e^{-(x/2\sqrt{Dt})^2} \quad (3.5)$$

where Q_0 is the initial dopant dose prior to diffusion (atoms/cm^2), D is the diffusivity (cm^2/s), x the diffusion distance (cm) and t the diffusion time (seconds).

A diffusion of this type trades surface concentration for diffusion depth and the final value for both is dependent on diffusion time with diffusion temperature simply acting as a rate modifier.

Practical implementation of the limited source diffusion is challenging as the actual quantity of dopant required is very small and as such special techniques are necessary to accurately monitor the dose. One answer is to use ion implantation which permits fine control over the dose [182] whilst the alternative is a two-step process combining both constant source diffusion and limited source diffusion.

3.1.2.3. Two Step Diffusion

The two step diffusion process is a practical implementation of the limited source diffusion process and is commonly used for silicon based device manufacture, both semiconductor and solar.

A short, low temperature, constant source diffusion is carried out initially. This “pre-deposition” forms a very thin layer of impurity in the surface of the silicon wafer. This layer is adequately shallow in the wafer as to be considered equivalent to a layer on the surface. The source is then removed leaving only the shallow diffused layer acting as the impurity supply and driven deeper into the wafer by a high temperature drive in step. If the drive in step is carried out in an oxygen rich atmosphere the highly doped region at the surface will be converted to SiO_2 which can then be removed by an etch step. Removing the most highly doped surface layer reduces the peak doping concentration, reducing damage caused by high doping concentration and in the case of solar cells improving the blue spectral response.

In commercial device manufacturing this process would be achieved with a dopant containing gas in a diffusion furnace. For instance, to achieve an n-type emitter on a p-type silicon substrate, phosphorus oxychloride (POCl_3) is often utilised as a phosphorus source. A nitrogen (N_2) carrier gas is bubbled through the POCl_3 liquid source before being flowed over the wafers to be doped at a temperature in the 700°C-900°C range. Here it decomposes into a layer of silicon dioxide (SiO_2) containing phosphorus pentoxide (P_2O_5) on the surface of the wafers. This material is commonly referred to as phosphosilicate glass (PSG). The disassociated chlorine (Cl) gas readily reacts with the majority of metals and aids in removing metallic surface contamination from wafers which would otherwise affect the p-n junction performance. After the required amount of phosphosilicate glass has been deposited the POCl_3 source is switched off to prevent further growth. The furnace temperature is then increased, driving diffusion of phosphorus atoms from the PSG source into the underlying silicon substrate. By controlling the POCl_3 flow rate and the diffusion temperatures, the doping concentration and junction depth can be modified.

3.2. Deposition and Processing Techniques

The systems used within this project to diffuse, deposit and post process the films and structures required to produce working cells are discussed below.

3.2.1. Rapid Thermal Processing (RTP)

The RTP system at LSBU is an AS-One 100 system designed and manufactured by Annealsys. The system consists of an all in one processing unit which contains the process chamber and all ancillary systems necessary to operate it. This is attached to a standard desktop PC from which “recipes” can be created and uploaded to the system and the processing monitored in real time.

The system uses an array of twelve 1200 W quartz halogen lamps for a total power output of 14.4 kW, fitted behind a quartz window. The process chamber is directly below the lamp chamber and is capable of supporting a single 100 mm silicon wafer on quartz pins. The system was originally intended to process whole wafers but is equally capable of processing smaller samples placed atop a sacrificial silicon wafer acting as a susceptor. The chamber is sealed by an O-ring arrangement and is capable of operating at atmospheric pressure, under a variety of process gases or at low vacuum. A simplified layout of the RTP chamber is shown in Fig 21.

Vacuum is provided by a Varian SH-110 dry scroll pump which contains no oil and as such is capable of handling oxidising and flammable gases without additional preparation. This was capable of providing a base pressure of better than 1×10^{-2} Torr. Process gases consist of research grade (99.9995%) nitrogen and Ultra Large Scale Integration (ULSI) grade (99.9999%) oxygen supplied via mass controllers (MFC) with digital control. This permitted one standard cubic centimetre per minute (sccm) resolution over a range of 40-2000 sccm providing excellent incremental control over the gas flow.

Temperature monitoring is carried out by an in-chamber K-type thermocouple and an 8-14 μm spectral range pyrometer. The thermocouple is generally used for lower temperature processing up to 500 °C whilst the pyrometer is useable up to 1100 °C.

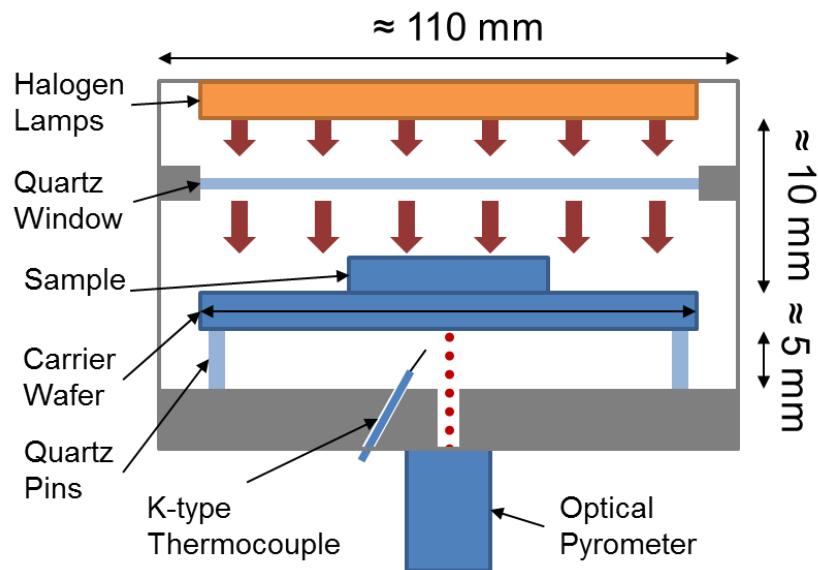


Fig 21. A simplified layout of the RTP system at LSBU

The system utilises "recipes" hosted on a controlling computer which allow accurate and repeatable processing to be carried out with high throughput capability. The technique is ideally suited to a variety of processes including; annealing contacts to form silicide

junctions, driving in spin on dopant with fine control over junction depth and high temperature defect annealing and crystallisation in deposited silicon films [183].

Generally speaking, it is possible to greatly accelerate processes that would take a substantial amount of time in a conventional furnace. A study was performed that involved aluminium contacts to p-type silicon which are traditionally sintered for approximately 60 minutes in the region of 500 °C in a tube furnace. It was found that the same process could be achieved in the region 60 seconds, also at 500 °C, in the RTP system. It was proposed that this was due to the difference in rate of delivery of thermal energy between the two systems. Whilst the tube furnace relies predominantly on conduction and convection to heat the sample, the RTP delivers energy predominantly in the form of infra-red radiation, and in a far more concentrated fashion (14,400 W from the RTP compared to 1200 W from the tube furnace).

It is also used to carry out proximity rapid thermal diffusion (PRTD) as a doping process. This process is a variation on gas phase doping and utilises a phosphorus oxide layer on a sacrificial wafer as a source. By heating the source wafer, phosphorus is diffused out of the oxide layer and across an air gap in a nitrogen stream before depositing on the surface of the samples to be doped, which are placed facing the source. Subsequent steps can then be carried out on the sample to drive in the dopant with fine control over the depth of the junction and activation of dopants [184].

In a similar fashion to the accelerated contact annealing discussed previously, the PRTD process permits diffusion to be undertaken at a far greater rate than that predicted by conventional diffusion calculations. This is believed to be due to the enhanced diffusion rate observed in the presence of a growing oxide. As oxidation also occurs at an increased rate under RTP conditions [185], this is the likely cause of the accelerated diffusion process.

Despite the obvious advantages RTP provides there are various issues which must be addressed for effective processing. The majority of these issues are related to control of process temperature and temperature uniformity.

Perhaps the most fundamental challenge is with the thermodynamics of the chamber itself. Unlike a conventional tube furnace where the system is operated with nominal thermal equilibrium throughout the chamber, the RTP operates as a “cold wall” system. To facilitate the rapid cooling of samples during processes the walls of the chamber are water cooled to provide a large thermal sink. However, this also results in a thermal gradient from the centre of the chamber to the outer edges. Attaining a level of thermal uniformity generally necessitates a short soak at processing temperature or carefully designed process ramps to

allow samples to reach thermal equilibrium. This may be problematic when short process steps are required or when processing temperature sensitive samples.

Another potentially problematic area for RTP processing is coupling of thermal energy from the lamp source into the sample. The predominant means of energy transfer in RTP is that of radiation and therefore the effective heating is dependent on the samples ability to absorb the various wavelengths produced by the halogen lamps. Highly reflective samples are likely to reflect a proportion of the incident light whilst very thin samples may simply transmit much of the applied radiation without being effectively heated.

With regard to temperature control, it was noted that during PRTD diffusion processes the carrier wafer used to support samples undergoing diffusion formed a layer of oxide as expected based on the oxidising process atmosphere. The carrier wafer was subsequently etched in hydrofluoric acid after each run to remove residual oxide and dopant at which point it was realised that this resulted in a thinning carrier wafer. To prevent pyrometer drift due to increasing optical transmission caused by the reduced wafer thickness, prior to subsequent diffusion runs it was necessary to recalibrate the pyrometer against the system thermocouple.

3.2.2. Tube Furnace

Many semiconductor processes require thermal steps to anneal, diffuse or passivate films and layers. A significant amount of this processing is carried out in a conventional high temperature tube furnace. The system at LSBU is predominantly utilised for electrical contact annealing post deposition to attain ohmic contacts. It is capable of operating at temperatures up to 1200 °C with a nitrogen purge for inert processing and wet or dry oxygen feed for growth of thermal oxides [186]. Samples are inserted and removed from the furnace tube on an automated loader which controls the insertion and withdrawal rate to minimise thermal shock.

Temperature control is carried out by a proportional, integral and derivative PID controller [187] with programmable ramp rates providing nominally repeatable processing from run to run. The large thermal mass of the system coupled with its slow response time necessitated careful tuning of the controller to prevent significant overshoot. This was particularly relevant when processing certain contacting schemes as excess temperatures could result in undesired interactions between materials and inferior contact formation. To mitigate this, values for P, I and D were recorded after auto tuning the controller for a certain temperature to attain repeatable thermal ramp profiles.

3.2.3. Sputter Deposition

Sputtering is a physical deposition process that relies on energetic ions and collisions with material surfaces to deposit thin films [188]. A typical sputtering system consists of a target of the material to be deposited which acts a cathode and a susceptor which forms the anode and carries the samples to be deposited on. A DC or RF power supply is then connected to the cathode to drive it whilst the anode may be grounded, floated or biased (Fig 22).

The system is contained within an evacuated chamber to which a sputtering gas, typically argon, is added and serves as a medium to support a glow discharge or plasma. The two types of glow discharge; DC and RF are discussed in more detail below.

3.2.3.1. DC Sputtering

When a DC voltage is first applied to the target, the small number of free charge carriers available results in only a small current flow. As the voltage is increased, the energy imparted to the charge carriers becomes sufficient to generate further carriers. This occurs by two mechanisms, ions colliding with the target release secondary electrons and ions colliding with gas atoms produce further electrons by impact ionisation. These processes accelerate rapidly resulting in a process referred to as avalanche ionisation. A point is reached where the electrons produced result in adequate ions to produce the same number of electrons again and the process becomes self-sustaining. It is at this point that the ionised gas begins to glow and the so called glow-discharge becomes visible between the cathode and anode. Initially this “normal glow” results in non-uniform bombardment of the target until sufficient power is applied to achieve a uniform current density across the surface of the cathode. Now the target is in an “abnormal discharge” region where typical sputtering takes place.

Ions within the glow discharge are accelerated toward the negatively charged target [189] where collisions between the ion and the target material result in the ejection of one or more atoms. The number of atoms ejected per incident ion is referred to as the sputter yield and is a metric for the efficiency of the sputtering process.

3.2.3.2. RF Sputtering

RF sputtering was developed to deal with the issue of sputtering non-conductive materials. To achieve a high enough current density to sputter a material, adequate voltage must be applied to achieve this current. Materials with high resistivities generally require unrealistic voltages ($> 1 \times 10^{10}$ V) to achieve the necessary current densities making DC sputtering unsuitable.

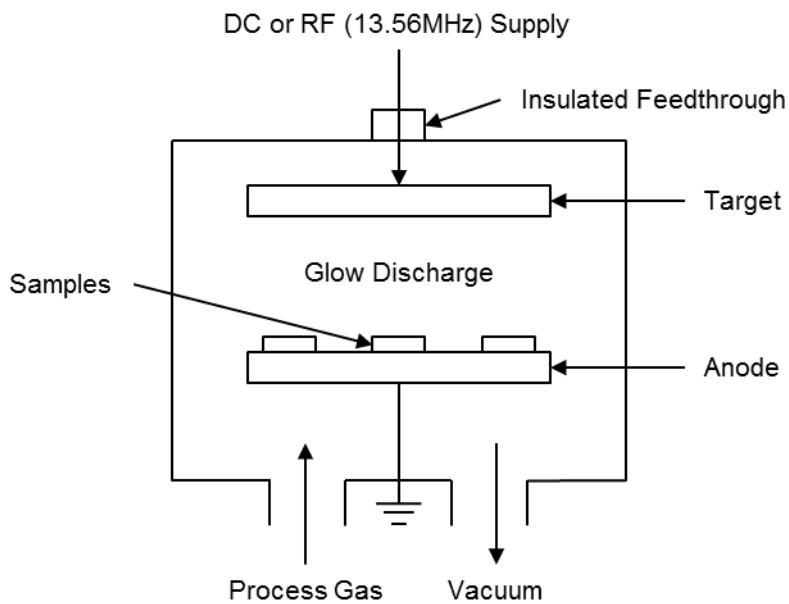


Fig 22. Simplified Sputtering Process Diagram. The target electrode is driven by a DC or RF signal which creates a potential between it and the anode which is grounded. The chamber is evacuated and a small amount of process gas is introduced to the chamber which is adequate to permit ionisation to take place and results in the glow discharge between the target and anode. Ions within the glow discharge are accelerated towards the target, sputtering off material which deposits on the samples placed atop the anode.

By applying an RF signal to the cathode, electrons in the glow discharge region gain adequate energy to cause ionising collisions with argon gas atoms which substantially reduces the requirement for secondary electrons from the target to sustain the avalanche ionisation. The process works because the target becomes self-biased to a negative potential. This negative bias results from the fact that electrons have a higher mobility than ions and are able to keep pace with the periodic reversal of the electric field maintaining the negative potential of the target. At this point the mechanism of operation is near identical to that of a DC driven target with positive ion bombardment sputtering off atoms for deposition.

It may be noted that the constantly changing potential creates the possibility of sputtering the susceptor as well as the target. The RF sputter system can be modelled as two capacitors, one the target and plasma sheath, the other the sample carrier assembly with the applied voltage shared between the two. Since the reactance of a capacitor is inversely dependant on capacitance, which is area dependant, the desired sputter region should be small compared to the rest of the system. This is commonly achieved by coupling the entirety of the chamber, with the exception of the target, to ground resulting in the largest possible

voltage being dropped across the target capacitance and achieving peak sputtering performance.

3.2.3.3. Magnetron Sputtering

The sputter system at LSBU is capable of both DC and RF target excitation but it occupies an additional sub category referred to as magnetron sputtering.

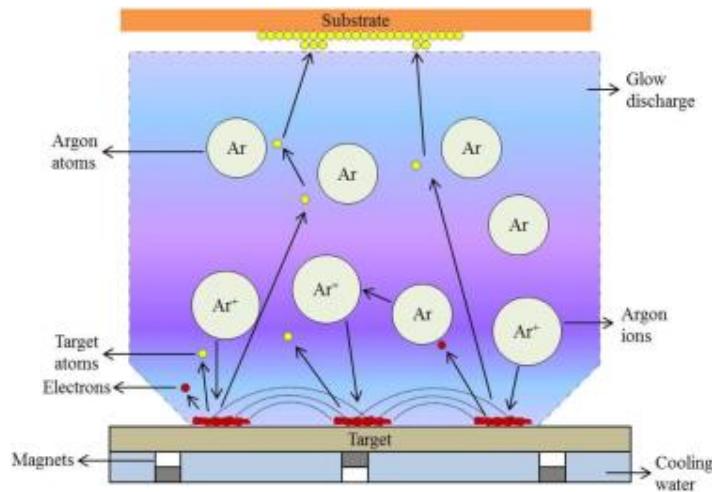


Fig 23. Magnetron Sputtering Configuration Diagram. The process is similar to that of RF sputtering but the addition of magnets behind the target causes electrons ejected at a non-normal angle of incidence to the target to orbit the magnetic field. This retains them within the plasma sheath rather than being lost to the grounded chamber surfaces which increases the ion generation rate and in turn the sputter yield. [190]

If one considers electrons ejected from the surface of the driven target, those ejected non-perpendicular to the surface have a high chance of being ejected out of the plasma sheath and lost to the grounded chamber walls. Electrons which are lost in this fashion are unable to generate further electrons by ionising collisions and reduce the efficiency of the sputtering process. By placing a magnetic field atop the electric field present between the target and susceptor, electrons which are ejected at a non-normal angle to the target now orbit the magnetic field in a helical fashion increasing the chance that they will remain in the plasma sheath (Fig 23).

Of course when considering RF magnetron sputtering, the ideal situation is that the majority of electrons are retained close to the target where they can enhance ion generation. This is achieved by creating a magnetic field which lies parallel to the target and perpendicular to the electric field, typically by placing magnets behind the target. Electrons ejected from the target are initially accelerated towards the susceptor but are then subjected to the magnetic

field lines which cause them to follow an orbit back towards the surface of the cathode. This localised area of intense electron presence and associated high ionisation cause a ring shaped “race track” in the target.

The enhanced ionisation attained by magnetron sputtering reduces the required process pressure required to sustain plasma and achieve a reasonable deposition rate. This has proven to be particularly beneficial for the deposition of the transmitting conductive oxide (TCO) aluminium zinc oxide (AZO) whose electronic properties are strongly dependant on deposition being carried out at low pressures (<15 mTorr).

3.2.3.4. Reactive Sputtering

A final sub-category of sputter deposition worthy of mention is reactive sputtering. Compound targets of oxides and nitrides often prove difficult to sputter effectively as the deposited film often does not possess the same stoichiometry as the target. By introducing oxygen or nitrogen to the argon sputter gas it is possible to reactively sputter oxides and nitrides of elemental targets with good control over the final stoichiometry achieved.

The sputter system at LSBU is a JLS Designs MPS 400 sputter system with four independently driven magnetron targets capable of sputtering in DC and RF modes. The chamber is pulled to a base pressure of 1×10^{-6} Torr by a Leybold Turbovac 1000c classic turbo pump backed by an Edwards 40 two-stage rotary vacuum pump. The susceptor is height adjustable, rotatable and may be heated by a carbon heater element or cooled by water. Gases are ULSI grade (99.9999%) argon, nitrogen and oxygen and are supplied via 0-100 sccm range mass flow controllers with 0-10 V input giving ≈ 1 sccm resolution.

Repeatability of deposited films for identical recipes was found to be generally good. Thickness was found to generally trend downwards over an extended period due to the race track effect on the magnetron targets. To correct for this, runs were periodically undertaken with known conditions to assess the film thickness variation and process parameters adjusted if necessary.

3.2.4. Electron Beam Evaporation (E-Beam)

E-Beam evaporation utilises a high energy, focused beam of electrons to heat and melt the source material to be evaporated which is held in a crucible [191]. The electrons are produced by a cathode filament electron gun with energies up to 20 keV and focused into a beam. The beam is then guided through 270° in an arc into the source crucible using a magnetic field at right angles to the electron beam. As the electrons energy is dissipated by the source, it is heated and the resulting evaporate is deposited onto the samples held

above. The E-Beam system at LSBU is a Kurt Lesker PVD 75 system with the ability to sequentially deposit up to four different metals (e.g. Cr, Ag, Au and Sn) onto an ambient temperature or heated substrate.

3.2.5. Thermal Evaporation

Thermal evaporation utilises a tungsten wire basket mounted between two insulated terminals, one grounded and the other connected to a low voltage, high current power supply. By supplying a voltage across the basket, a large current is drawn resulting in a resistive heating effect. By this method, materials with melting points up to ≈ 1800 °C can be evaporated at high deposition rates [192].

The system at LSBU is a Moorfield Minilab with four evaporation terminals allowing sequential deposition of different source materials, such as Al, Ti and Ag. It is fitted with a rotary pump to reach low vacuum and a turbomolecular pump to attain a high vacuum in the 1×10^{-6} Torr range. By depositing at high vacuum the required temperature to increase the vapour pressure of many materials above the chamber pressure is significantly reduced and the purity of deposited films is greatly enhanced.

3.2.6. Film Thickness Monitoring

Both the E-Beam and Thermal evaporator systems make use of a film thickness monitor. This employs a crystal oscillator mounted within the deposition chamber and in line of site of the source. The crystal has a resonant frequency dependant on a variety of factors, with density being particularly relevant. As material deposits on the crystal from the source, the mass of the plate increases and as a result its resonant frequency falls. The change in frequency as a result of increasing mass can be described by the Sauerbrey Equation [193]:

$$df = -\frac{f^2}{C_{pf}} \frac{dm}{A} \quad (3.6)$$

Where C is the frequency constant which is defined as 1656 kHz/mm for AT cut quartz as commonly employed in crystal oscillators, d is the film thickness, m the mass and A the area of the oscillator. From this it is possible to get an indication of the measurement resolution achievable by this method. If a standard 6 MHz crystal is assumed, then as a shift in frequency of 1 Hz is easily discernible, this equates to a mass of aluminium of 1.24×10^{-8} g which for a 1 cm^2 crystal oscillator is equivalent to a film thickness of 4.6×10^{-2} nm [194].

As the film thickness monitors in use at LSBU are designed to monitor film deposition in real time, the hardware measures the change in frequency with respect to time and displays both

thickness and deposition rate. Prior to use it is necessary to enter the density of the material being evaporated and its z-ratio to allow the instrument to measure correctly. The z-ratio corrects the acoustic impedance mismatch between the crystal oscillator and the film deposited upon it due to the two films having different densities and acoustic velocities [195]. Without this value, as the film thickness increased the measurement error would be steadily compounded.

3.2.7. Chemical Vapour Deposition (CVD)

Chemical vapour deposition is a process by which a volatile source material may be reacted with other gases to atomistically deposit a thin film. By this method a wide variety of films and coatings of metals, semiconductors and compounds may be produced in a crystalline or amorphous state, possessing high purity and finely controllable properties. Additionally, CVD allows for variable stoichiometry of deposited films permitting different compounds to be deposited [196].

There are a number of possible chemical reactions that may occur under the umbrella of CVD. These include; pyrolysis, reduction, oxidation, formation of compounds and disproportionation. Of these methods, only pyrolysis and oxidation are relevant and discussed in further detail here.

Pyrolysis describes the thermal decomposition of gaseous species atop a heated substrate. A commonly employed example of this process is the decomposition of Silane (SiH_4) to form amorphous or polycrystalline silicon films by the reaction:



This reaction generally occurs at temperatures exceeding 650 °C which places restrictions on the materials upon which it may take place. It is also possible to deposit silicon epitaxially atop a silicon substrate by this method but requiring temperatures in excess of 1000 °C to attain this reaction.

The other CVD technique utilised is oxidation. Deposited silicon and indeed single crystal silicon which has undergone processing is left with a crystal lattice possessing dangling bonds at the surface. These dangling bonds have high surface energy which leads to increased recombination and a corresponding loss of performance in devices. To reduce these losses, surfaces may be oxidised to form silicon oxide which caps and passivates the dangling bonds. As with pyrolysis, this process requires a heated surface to decompose the molecular oxygen to elemental oxygen atoms which may bond with the silicon surface.

3.2.8. Plasma Enhanced Chemical Vapour Deposition (PECVD)

PECVD is a class of Chemical Vapour Deposition (CVD) which reduces the thermal energy required to allow pyrolytic deposition from the gas phase. Depositing silicon from a precursor such as silane (SiH_4) under conventional CVD generally requires a substrate temperature in excess of 650 °C, increasing to over 1000 °C for epitaxial silicon growth. This precludes the use of many substrates proposed for use in thin film cells such as glass and plastics.

The use of a plasma generated by an RF source at 13.56 MHz allows the dissociation or cracking of silane into its component parts. This cracking prior to deposition allows silicon formation on a substrate at far lower temperatures than conventional CVD [197].

The system at LSBU employs an 800 W RF source with automated matching unit to drive the plasma, utilising the sample holder as the antenna and the chamber walls as the ground.

3.2.9. Electron Cyclotron Resonance Chemical Vapour Deposition (ECRCVD)

ECRCVD is a variation on PECVD. Whilst it still utilises a plasma to reduce the substrate temperature required for deposition, the excitation frequency is shifted to the microwave region of the electromagnetic spectrum at 2.45 GHz. In the case of ECR, the plasma is struck in a chamber above the substrate and guided toward it using a magnetic field. As the ions and the electrons formed by the plasma are charged particles they react to both electrical and magnetic fields. In the case of the magnetic field, electrons travel in a circular motion around the field lines. If they are additionally exposed to an electric field they will continue to orbit the magnetic field lines as well as drifting perpendicular to the electric field. This motion gives rise to a resonant condition from which ECR derives its name [198].

The ECR system at LSBU is of bespoke design and in its original form was of the divergent field type [199]. This utilised a wave guide to channel microwave energy from a source to a quartz window which acted as a feed through to the chamber. It also used a pair of electromagnets with independent power supplies that allowed the shape and position of the magnetic field to be tuned.

It has subsequently been modified to use a new microwave supply and a more compact electromagnet. The microwave generator is still mounted atop the system but the output is now coupled with an antenna that distributes the microwave energy into the top of the upper portion of the vacuum chamber via a dielectric cup (quartz). The cup acts as a feed through and allows the microwave energy to pass into the chamber whilst maintaining the high vacuum necessary for processing. The microwaves excite the gas injected into the upper portion of the chamber giving rise to plasma which is encapsulated by the electromagnet

ring. The magnetic field cuts across the gas discharge volume and produces a cross section which is referred to as the ECR zone. It is possible to vary the position of this zone by varying the electromagnetic field strength, which in turn produces different plasma streams at the sample holder. Prior to reaching the sample holder the plasma stream is passed through a gas showering ring which supplies process gases.

By biasing the substrate holder in the path of the plasma stream with an RF field it is also possible to vary the energetics of the ions striking the samples.

3.2.10. Reactive Ion Etching (RIE)

The ECR system can also make use of plasmas formed of reactive gases to carry out reactive ion etching. Notably, etching was in fact one of the original purposes behind the development of ECR for the semiconductor industry [200].

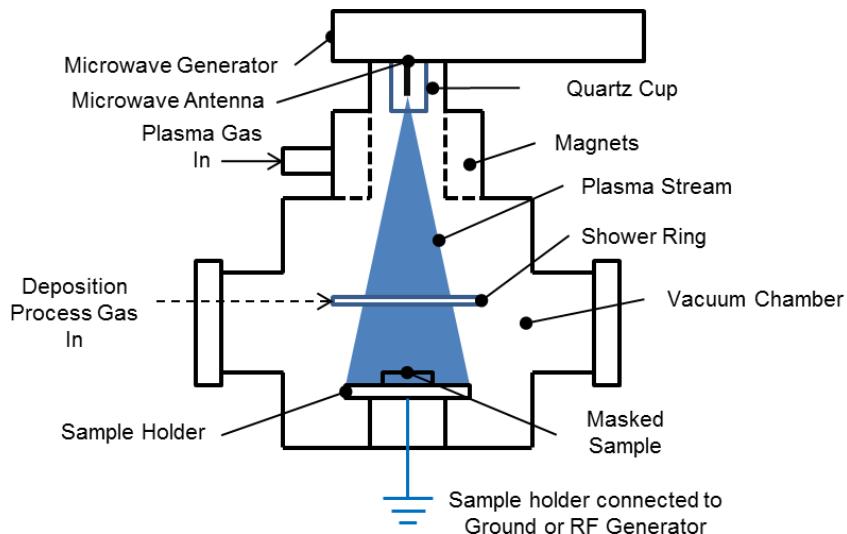


Fig 24. Simplified diagram of ECR-CVD system. The microwave energy is coupled into the top of the chamber through a quartz cup where it ionises a stream of gas creating a plasma. This plasma is contained within a magnetic field which guides a stream of plasma down the chamber through a gas shower ring where it interacts with the process gas, breaking it down prior to it reaching the sample holder.

This process utilises sulphur hexafluoride which is dissociated in the plasma stream to form elemental fluorine. This reacts with silicon, etching it and forming silicon fluoride (SiF_4). When carried out under ECR conditions with an RF biased sample carrier it is possible to achieve a high etch rate with reasonably anisotropic etch conditions resulting from the uniform directionality of the reactive ion stream. A simplified diagram of the LSBU ECR system is shown in Fig 24.

3.2.11. Deep Reactive Ion Etching (DRIE)

Deep reactive ion etching (DRIE) is a development of conventional RIE, capable of achieving very high levels of anisotropy resulting in deeply etched high aspect ratio features. The most common variation of DRIE is the Bosch Process, named after the company that developed it [201], also known as pulsed or time-multiplex etching. This process repeatedly cycles between two modes, etching and passivation, to attain near vertical features over significant depths. During the etch mode, the masked substrate is exposed to a conventional plasma etch, whose primary action is by chemical interaction, although some predominantly vertical ion bombardment does occur. Subsequently, during the passivation cycle, a chemically inert layer is deposited which masks all exposed surfaces. During the following etch cycle, the side walls of features are protected by the passivation layer but the directional ions which bombard the substrate sputter the passivant on horizontal surfaces and expose them to the gas phase etchant. By repeatedly cycling these etch and deposition steps a large number of shallow isotropic etches take place only at the base of masked features. This process leads to a characteristic faceted side wall with a frequency dependant on the cycle time (Fig 25).

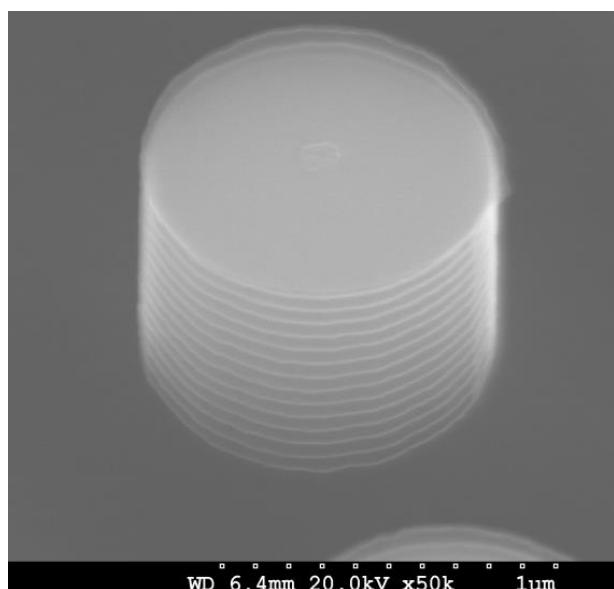


Fig 25. An SEM image demonstrating the characteristic faceting which results from the DRIE etching process

3.3. Characterisation Techniques

The systems used to characterise samples and cells optically and electronically are discussed in the following section.

3.3.1. Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) [202] utilises an electron gun to produce a stream of electrons from the cathode which by virtue of their negative charge are attracted towards an anode, atop which the sample to be imaged is mounted. By rastering the beam across the sample and analysing the reaction between the electrons and the sample an image can be rendered. There are two common means by which the electron beam may be produced, thermionic emission and field emission both of which use a filament as the electron source. A thermionic emission gun heats the filament to lower the work function of the filament material allowing electrons to be readily drawn off by an electric field. The field emission gun places the filament at a voltage potential to a first anode which overcomes the work function of the filament material so electrons may be drawn off it. The voltage potential between the gun and the first anode is the extraction voltage and is typically 3-5 kV. A second anode beyond the first has a variable potential, typically between 500V-30 kV described as the acceleration voltage which defines the energy with which electrons are accelerated towards the sample. Field emission guns have a longer life span than thermionic emission guns but are inherently more unstable with emission variation during an initial warm up period.

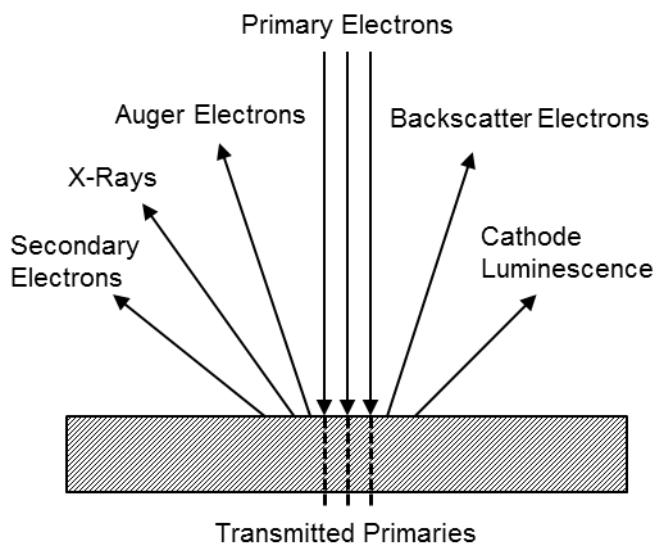


Fig 26. Electron interactions with samples which are undergoing SEM analysis. The depth at which the primary electrons interact with the material dictates the type of emission from the sample.

The SEM at LSBU is a Hitachi S-4300 and is of the field emission type. To mitigate the effects of emission intensity falling during initial operation, the system was allowed to warm up for a period of time and the emission voltage monitored during use to minimise the effect on data collection.

After emission the electrons are focused through a condenser and objective lens to adjust the beam spot size and focus it on the sample respectively. The distance the electrons travel from the objective lens to the surface of the sample is described as the working distance and for best resolution should be maintained at the smallest distance possible. It is also important that a constant distance be maintained when imaging different samples for comparison.

Between the objective lens and the sample, the electron beam is rastered over the sample surface by a pair of magnetic coils. These primary electrons, upon impacting the surface, transfer their energy into the surface in a tear drop shaped area of interaction [203]. This causes multiple electron excitations resulting in the emission of secondary electrons, back scatter electrons and X-rays depending on the depth of the electron interaction in the sample (see Fig 26).

The secondary electrons, which result from inelastic scattering interactions with probe beam electrons and originate within a few nanometres of the surface, are those most commonly used for SEM imaging. They are detected by an Everhart-Thornley detector which uses a combination of a phosphorus screen or scintillator and a photomultiplier [204]. The emitted electrons are first collected by attracting them towards an electrically biased grid (≈ 400 V) and then further accelerated towards a biased scintillator screen (≈ 2000 V). The electrons now possess sufficient energy to promote cathodeluminescence in the scintillator which is measured by a photomultiplier. The output from the photomultiplier is then rendered as a two dimensional variable intensity image which is displayed to the operator.

Backscatter electrons are high-energy electrons from the electron beam that are scattered out of the specimen through elastic interaction with the constituent atoms. Heavy elements with large atomic numbers promote higher levels of backscattering than their low atomic number, light element counterparts. The result of this is that the heavy elements appear brighter when imaged. This contrast permits identification of differing material areas on samples with varying chemical compositions.

In addition to standard backscatter imaging, the SEM is capable of electron backscatter detection (EBSD) permitting examination of the crystallographic structure of sample. The sample is placed at a highly tilted angle towards the EBSD detector which consists of a phosphor screen and CCD camera. As the probe beam produces backscatter electrons, some will escape near to the Bragg angle [205] and produce Kikuchi bands [206] which relate to the crystal lattice planes. By indexing these bands against the Miller indices of the diffraction plane which produced them it is possible to define the crystal structure of the material using a series of look up tables. It is important when applying this technique to

ensure samples are consistently orientated to ensure the orientation of the measured bands is accurate.

X-ray energy dispersive spectroscopy (EDS) is a technique used for the elemental or compound analysis of a sample. When an atom in the material is struck by the high energy electron beam of the SEM, an electron in the atom's lower electron shell may be excited and ejected leaving the atom in an ionised state. To return to a stable condition, an electron from a higher energy shell falls to the lower shell and the excess energy may be released in X-ray form. The EDS detector characterises the number and energy of X-rays produced by the sample. As the X-ray energy is dependent on the difference in energy between the atoms two electron shells and of the structure of the element from which they were emitted, the composition of the sample under analysis may be determined. It is also possible with the use of analytical standards to quantify the stoichiometric composition of the sample [207].

As the SEM relies on a beam of electrons for imaging, it is important that samples undergoing analysis do not become charged as this can result in distortion or image drift during high resolution image capture, undertaken at a slower raster rate. Conductive samples such as metal films or highly doped silicon were often adequately contacted to the sample holder either via conductive paint or a carbon pad. Non-conductive samples pose more of a problem and it was occasionally necessary to sputter a thin (<5nm) layer of gold onto the surface to produce an adequate conductive path whilst preserving surface features [208].

3.3.2. Atomic Force Microscopy

Atomic force microscopy allows analysis of surfaces with a theoretical resolution on the atomic scale [209]. Fundamentally the system consists of four key components, a cantilever with a stylus at one end, a crystal oscillator which vibrates the cantilever at a known frequency, a laser which reflects off the cantilever into a detector and a PC and interface that control the AFM and interpret the data it produces.

The system operates in one of two modes, contact and tapping (Fig 27). Contact, as the name suggests, effectively drags the stylus across the sample and maps the surface based on the deflection of the cantilever. Tapping mode employs the crystal oscillator to vibrate the cantilever in the region of its resonant frequency with an amplitude on the order of 100-200 nm. When the tip is in close proximity to the surface, Van der Waal [210] and electrostatic forces act upon the cantilever causing a reduction in the amplitude. The feedback controller adjusts the height of the cantilever and oscillator assembly to maintain constant amplitude at the tip. The tapping mode profile of the surface, therefore, is made up

of the many discrete contact points with the surface without the lateral forces applied by dragging the stylus across the surface. This makes the method ideal for fragile surface samples which might be damaged by or difficult to measure with contact AFM. The system at LSBU is a Veeco Multimode scanning probe microscope which is normally run in contact mode.

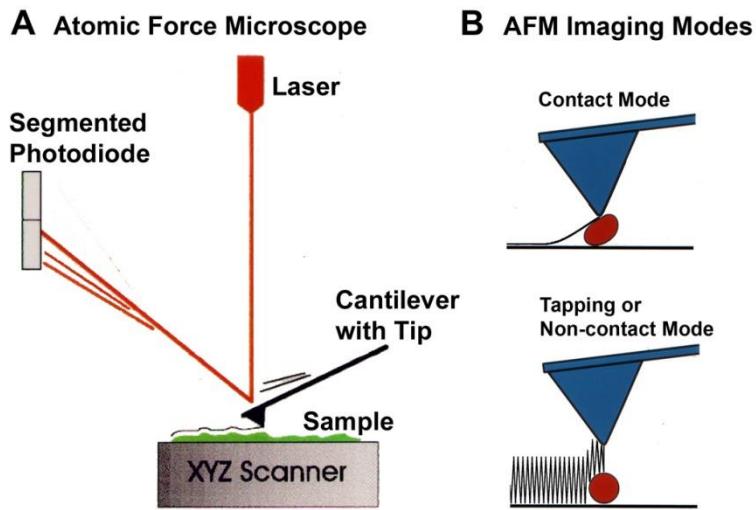


Fig 27. Fundamental operation of an AFM. In contact mode the tip is effectively drawn across the surface and the deflection upon reaching an obstacle is measured. In Tapping mode the tip is vibrated at high frequency and the effect on amplitude of Van der Waal forces monitored to adjust the tip position without contacting the sample surface. [211]

3.3.3. Stylus Profilometry

The Vecco Stylus Profilometer at LSBU can be used for a variety of purposes. Chiefly among these is step profiling to allow characterisation of a deposited films thickness and average surface roughness by averaging the variation of change in height over a film's surface [212]. The profilometer utilises a stylus mounted at the end of a cantilever whilst the other end is monitored by a piezo crystal for movement. By drawing the stylus across the surface of a sample and resolving the signals produced by the piezo crystal, it is possible to discern steps in the low Angstrom range. An example of the produced data is shown in Fig 28.

The systems resolution is dependent on the set vertical range of the cantilever; 1 Å at 65 kÅ, 10 Å at 655 kÅ and 40 Å at 2620 kÅ, although it was found that 50 Å-100 Å was the minimum realistic value which would be reliably discerned from background noise. Evaporated films generally exhibited cleanly defined steps, however, very thin plasma

deposited films could often prove difficult to discern from background noise due to their non-abrupt steps. In some cases this could be overcome by multiple measurements and analysis of the average surface roughness either side of the step to attempt to extract the step height from the noise.

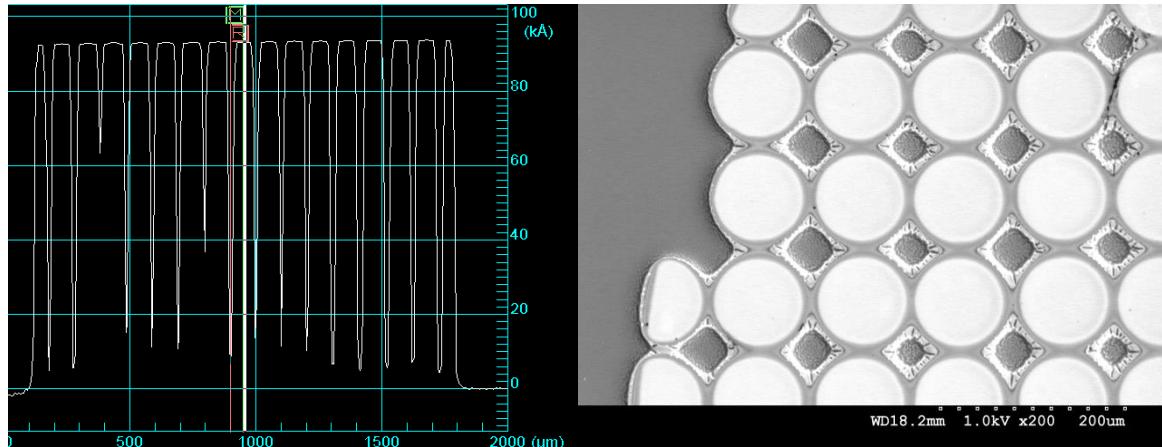


Fig 28. Stylus Profilometry data plot and an SEM image of the sample from which the measurements were taken.

The main limitations to accurate measurement were the ability to discern small or unclearly defined steps from surface roughness and cantilever noise caused by background vibration. This issue is partly mitigated by mounting the system on an air table which floats the surface on a cushion of air to reduce vibration coupling from external sources.

3.3.4. Raman Spectroscopy

Raman spectroscopy operates by focusing a beam of monochromatic light (usually from a laser) upon a sample and capturing the reflected light which is scattered inelastically [213]. The light interacts with the molecules or more specifically the electron cloud and bonds of the molecules within the material lattice and the returning light is captured and analysed.

Upon impact with a molecule, the laser light excites the molecule to a virtual energy level. When it reverts back to its ground state, it emits a photon and the molecule returns to a different vibrational state. The change in energy between the initial state and the resulting state produces a change in frequency of the emitted photon from the impacting photons wavelength. If the molecule is more energetic post excitation, the emitted photon energy will be of a lower frequency to maintain the energy balance of the system and is described as Stokes shifted [214]. Conversely, if the molecule is less energetic post excitation then the emitted photon frequency will be higher and is described as anti-Stokes shifted.

By analysing the change in energy experienced by the scattered photons it is possible to infer the various vibrational modes of the sample which allows the inference of the composition and crystallinity of samples. This is particularly useful when considering silicon samples as it allows the proportion of amorphous, to microcrystalline, to monocrystalline silicon to be analysed non-destructively and is demonstrated in Fig 29. The blue trace is the Raman response of a single crystal silicon wafer sample with a strong band at 520 cm^{-1} . Compare this to the red trace of CVD deposited silicon with fractions of amorphous silicon indicated by the broad band response around 480 cm^{-1} . The CVD silicon is deposited atop a silicon substrate and is adequately thin that the underlying monocrystalline silicon is also picked up resulting in the 520 cm^{-1} peak.

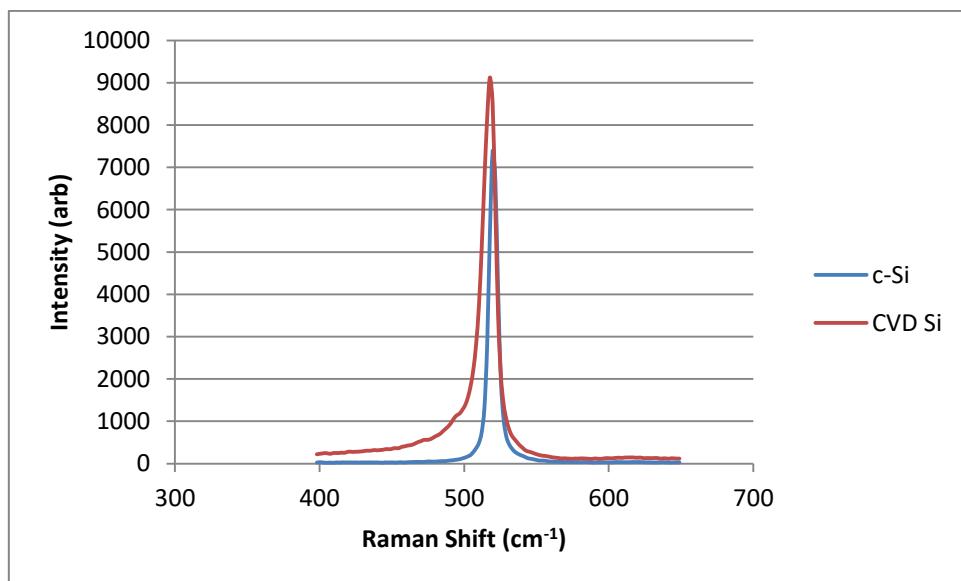


Fig 29. Typical c-Si and CVD Si Raman spectra. Both exhibit a strong peak around the 520 cm^{-1} mark as the CVD Si is deposited on a Si substrate and is insufficiently thick to prevent laser interaction with both materials hence the present but weaker signal.

Pre and post annealing Raman spectroscopy of deposited films can give insight into the effect on the lattice and any strain that may be added or removed from the film as a result of such treatments [215].

The system at LSBU is a Renishaw Ramascope operated in conjunction with a 50 mW argon laser at 488 nm providing the monochromatic light source.

3.3.5. I-V Analysis of a PV Device

I-V analysis serves multiple purposes as a characterisation tool [216]. The most common use is for cell testing as from an I-V curve it becomes possible to calculate the cells efficiency, fill factor and infer the quality of the junction.

At LSBU the I-V measurements are taken utilising a Keithley Instruments 2042 Sourcemeter controlled by a bespoke National Instruments Labview VI allowing specific sweeps to be configured and the results recorded. Test cells are measured in conjunction with a Photo Emission Tech SS80A class A solar simulator which accurately recreates AM1.5G illumination conditions of 1000 W/m^2 with the correct wavelength profile. They are additionally mounted on a Bentham water cooled, Peltier temperature controlled vacuum stage which secures and maintains samples at the standard 25°C required for cell measurement. The system is calibrated prior to each use with a standard reference cell from the Fraunhofer Institute to ensure test conditions are repeatable.

Additionally, I-V analysis has been used to test the performance of metal semiconductor contacts. This provides both an indication of whether the junction formed is Ohmic or Schottky and allows the specific contact resistance to be calculated by application of the transmission line method.

3.3.6. Spectrophotometry and Quantum Efficiency

The Varian Cary 500 Scan spectrophotometer at LSBU is a multipurpose optical characterisation device. It is capable of producing and detecting light from the UV range, through the visible and into the short-wave infrared region (175-3300 nm). It employs a pair of lamps (tungsten and deuterium) and a series of shutters and gratings to produce monochromatic light in nanometre steps. Light is passed through the system with one beam being fed directly to a detector as a reference measurement and then second being directed to the measurement area. This beam can then be guided through various fixtures depending on the measurement requirement before returning to a second detector. This allows transmission and reflection to be measured and as a result absorption can be inferred [217].

Its most common use is the measurement of transmission and reflection properties of deposited films and structured surfaces. For the purpose of making these measurements, an integrating sphere module is fitted to the system which facilitates the collection of both specular (reflection at normal angle to the surface) and diffuse (reflection at any other angle) light.

The Bentham Instruments PVE300 system at LSBU is a multipurpose optoelectronic characterisation tool. It is capable of carrying out reflection and transmission measurements as well as photovoltaic spectral response measurements. It is equipped with a broadband light source and stepping monochromator which produce a single nanometre step capable probe beam. This is coupled with a calibrated silicon reference diode connected to a pre-

amplifier and lock-in amplifier capable of measuring in the nanovolt range. The system control and measurements are controlled by over GPIB on an attached PC.

Its primary use is for quantum efficiency measurements of test cells. Quantum efficiency is a measurement of the generation and collection of carriers in a cell in relation to the incident photons [218]. It includes two variations, external quantum efficiency (EQE) and internal quantum efficiency (IQE). EQE is the ratio of charge carriers collected to the number of photons incident on the cell whilst IQE is the ratio of charge carriers collected to the number of photons that are actually absorbed by the cell (i.e. not reflected or transmitted). Therefore the PVE300 measures EQE, and IQE is then calculated by subtracting the measured reflection and transmission of the cell. The IQE curve then indicates the generation efficiency of the cell on a wavelength dependant basis.

3.3.7. Suns- V_{oc}

The Sinton Suns- V_{oc} is an opto-electronic characterisation tool that facilitates semiconductor device analysis at various stages throughout development [219]. It consists of a temperature controlled sample stage with a contacting probe, a mounted xenon lamp flash with neutral density filters and a PC interface for control and monitoring.

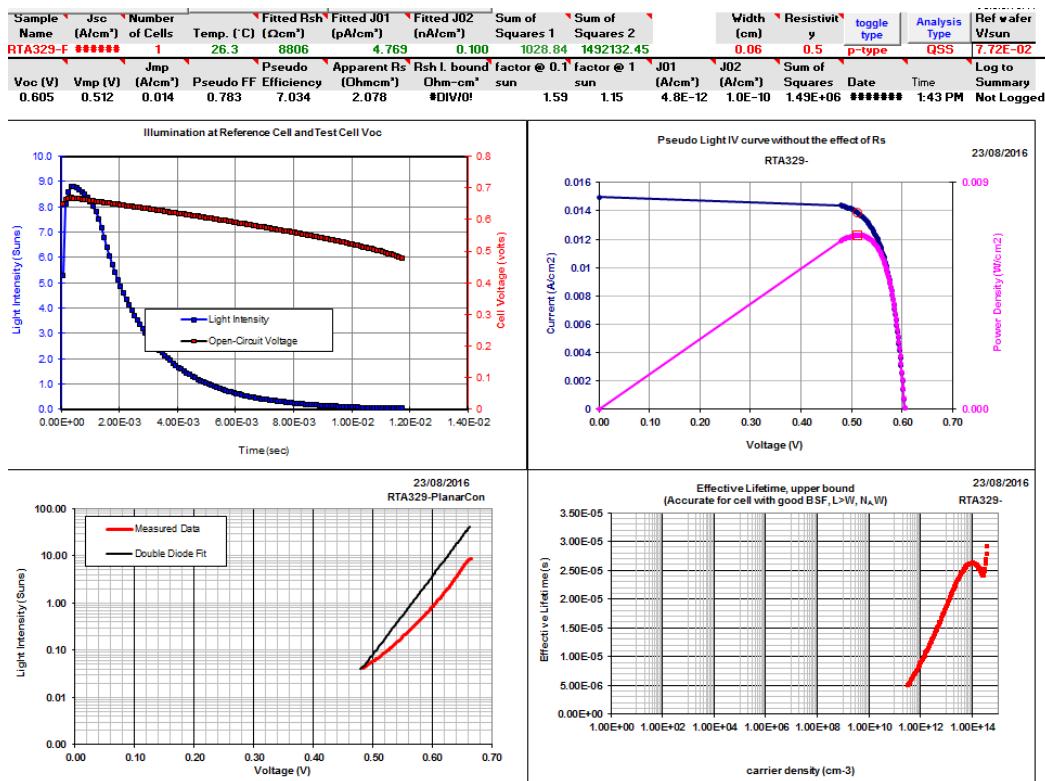


Fig 30. Data output by Suns- V_{oc} system. The available information includes predicted device parameters, pseudo I-V curve, diode model fit and estimated carrier lifetime.

The sample to be measured is momentarily illuminated, with the quasi steady-state open circuit voltage (V_{oc}) being measured as a function of decreasing light intensity from the flash. As V_{oc} is directly measured, rather than the short-circuit current, it is generally accepted that the contact of a sharp tipped probe is an adequate contact. This permits testing of unfinished devices to monitor parameters such as junction formation without the need to apply metallised contacts prior to measurements being made.

To obtain implied or pseudo I-V curves from the Suns- V_{oc} technique, a value for the short circuit current density (J_{sc}) is required. Unless a complete contacted cell is produced and characterised under a conventional AM1.5(G) solar I-V tester then this must be approximated. As the majority of samples investigated by this technique are incomplete this is generally the case. Approximations are generally based on measured J_{sc} values from a variety of previously produced complete test cells similar to devices under test. Even with an accurate value for J_{sc} the I-V curve extracted from the Suns- V_{oc} data would be at the upper bound for performance as the technique does not take into account the series resistance of the cell. Indeed, by comparing the Suns- V_{oc} of a cell and the measured I-V curve a reasonably accurate value for series resistance may be determined. A typical output produced by the Suns- V_{oc} system is shown in Fig 30.

The system is capable of predicting a number of device properties based on the response to the incident light impulse. These include fill factor, efficiency, and series and shunt resistance. In addition, a number of plots are produced which provide information about the device. Top left is the voltage response of the cell to the light pulse plotted against time whilst top right is the predicted I-V curve of the device. Bottom left is a plot of the measured voltage vs intensity and a fit of the double diode model to the data. An ideal diode produces a nominally straight line and therefore an indication of the device's performance may be established simply by comparing the measured data (in red) to the double diode fit (in black) with a close fit suggesting a better device. Bottom right is the density vs lifetime data which gives an indication of device performance as longer lifetimes are generally indicative of greater current generation. Whilst the accuracy of actual values produced by the system rely on a high quality back surface field at the rear of the device, even absent this, the data can be usefully used as a comparison between devices.

3.3.8. Four Point Probe

The four point probe technique is used to measure the resistivity of materials and commonly semiconductors. The system in use at LSBU is a Jandel RM3 and consists of two parts. The first is a measurement station which consists of four equally spaced tungsten tips which may be lowered onto the sample surface. The second is an interface consisting of a high impedance current source which supplies the outer probes and a voltmeter which measures the voltage resulting from the current flow (Fig 31).

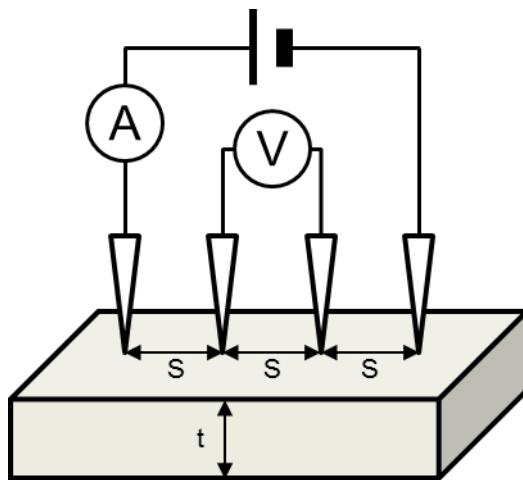


Fig 31. Four Point Probe measurement configuration. Current is sourced from the outer probes and the resulting voltage is measured by the inner pair of probes.

For measurements of a bulk sample where the sample thickness t is much greater than the probe spacing s the current spreading from the outer probe tips is modelled as a sphere and the resistivity is calculated as [220]:

$$\rho = 2\pi s \left(\frac{V}{I} \right) \quad (3.8)$$

However, in the majority of cases the thickness of the sample will be significantly less than that of the probe spacing (thickness, $t \ll s$) and a correction factor a must be applied as the current will spread out in rings rather than in sphere:

$$\rho = a 2\pi s \left(\frac{V}{I} \right) \quad (3.9)$$

Where a is the thickness correction factor as plotted in Fig 32.

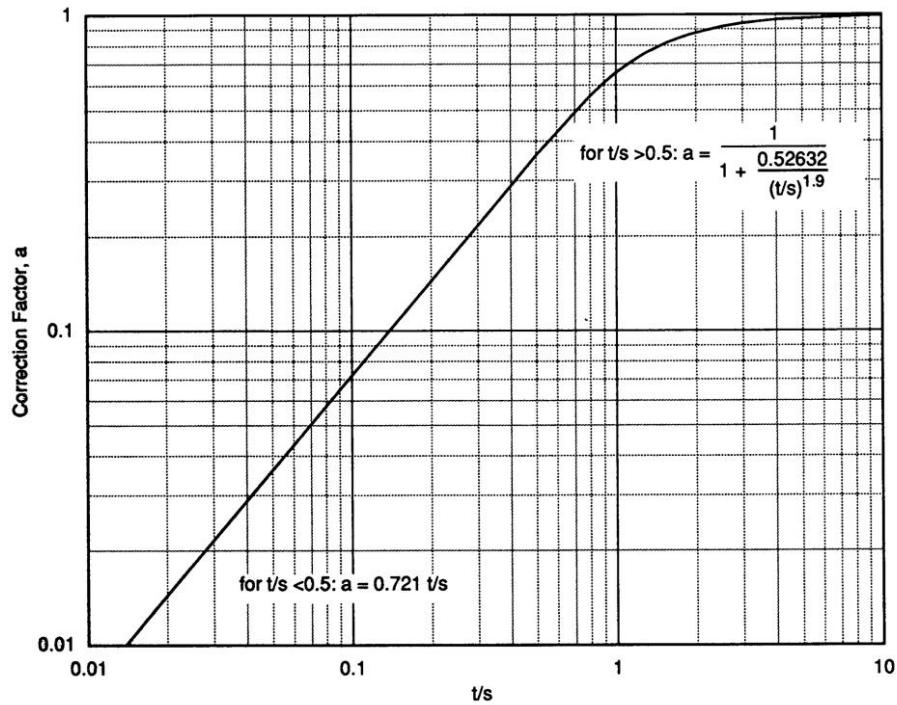


Fig 32. Thickness correction factor plot. Commonly required when the sample being measured is a deposited film and is therefore significantly thinner than the spacing between the measurement probes. [221]

As the plot is log-log the equation for the line must be in the form:

$$a = K \left(\frac{t}{s}\right)^m \quad (3.10)$$

Where K is the value of a when $t/s = 1$ and m is the slope. Inspection of the plot indicates that $m = 1$ and K is 0.72 by extending the linear region to the point where $t/s = 1$. Therefore for films where $t \leq s$ then $a = 0.72 t/s$.

By substituting this back into equation 3.10 we find:

$$\rho = 4.53t \left(\frac{V}{I}\right), (t/s) \leq 0.5 \quad (3.11)$$

As all samples that are to be measured will satisfy this relationship the above equation is a suitable means to calculate resistivity.

The four point probe system applies the correction factor automatically to the measured voltage; however, the system does not have a value for the film thickness. As such, it displays sheet resistance in ohms per square (Ω/\square) which models a thin film as a 2D sheet. The resistivity can then be calculated from this value by multiplying by the film thickness.

3.3.9. Transmission Line Method

The transmission line method (TLM) is a technique used to assess the contact resistance between a metal and a semiconductor material [222]. An array of identically sized ohmic contacts is prepared on the semiconductor with various spacings as shown in Fig 33.

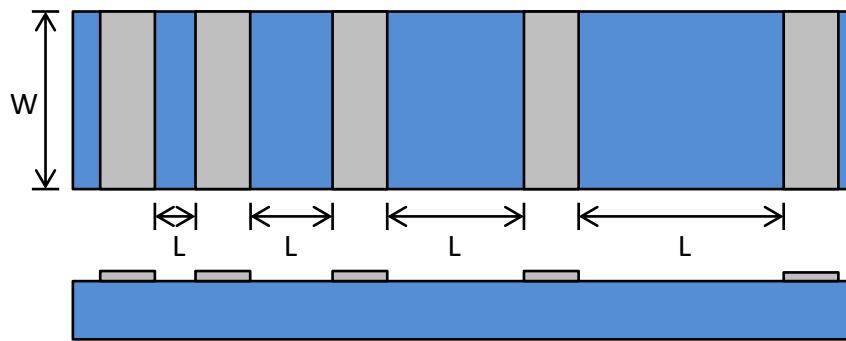


Fig 33. TLM Contact Arrangement

A voltage is applied across each pair of adjacent metal contacts and the resulting current flow measured to calculate the resistance. The measured resistance will consist of three components, the resistance between the first metal contact and the semiconductor, the resistance of the semiconductor itself and the resistance between the semiconductor and the second contact. Plotting the measured resistance against the inter-contact spacing should result in a straight line with positive slope. If the line is extended to $L=0$ the resistance of the two contacts alone can be extracted. The contact resistance is then simply this value divided by two [223].

This value is, however, a simplification as it does not take into account the fact that the contact pads are not at the ends of the semiconductor material but rather are on the surface. The result of this is that the current flow is greatest at the edges of the contacts nearest to each other with the current flow dropping off towards the edges furthest apart [224]. This phenomenon is referred to as “current crowding”.

To attain a more accurate value for contact resistivity it is necessary to find a value for transfer length (L_T) which describes the average length that an electron (or hole) travels within the semiconductor below the contact before transitioning into the contact itself. It is given by [225]:

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \quad (3.12)$$

where ρ_c is the contact resistivity and R_s is the sheet resistivity of the underlying semiconductor.

The effective area of the contact can therefore be described as L_T multiplied by the contact width W . The contact resistance is then given by:

$$R_C = \frac{\rho_C}{L_T} = \frac{R_S L_T}{W} \quad (3.13)$$

The most convenient way to obtain the value for L_T is in fact from the TLM plot by extrapolating the linear fit back to the x-axis, where the intercept value is equal to $-2L_T$.

3.3.10. Hall Effect

The Hall effect, as discovered by Edwin Hall in 1879, describes the resulting voltage change measured across a current carrying conductor when placed in a magnetic field perpendicular to the current flow [226]. In the absence of a magnetic field, charge carriers in a conductive material typically flow in a point to point fashion between contacts. When exposed to a perpendicular magnetic field the carriers experience a bending force, called the Lorentz force, dependant on their polarity and that of the magnetic field. This results in an accumulation of carriers on one side of the material and a corresponding depletion on the opposite edge. This continues until such a time that the charge separation opposes further carrier flow. The measured voltage is referred to as the Hall voltage and is dependent on the density of and mobility exhibited by the charge carriers (electrons and holes) in the current carrying material (Fig 34).

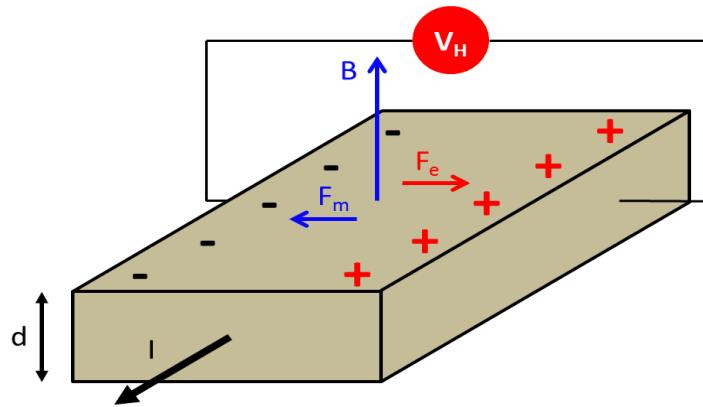


Fig 34. Hall effect principle for negative charge carriers (i.e. an n-type sample)

The Hall voltage across a sample can be calculated by equation 14:

$$V_H = \frac{-IB}{nte} \quad (3.14)$$

Where I is the current applied across the conductor, B is the strength of the applied magnetic field, t is the thickness of the conductor, e is the charge on an electron and n is the charge carrier density. Therefore by measuring the Hall field of a sample with known thickness and in a specific magnetic field the carrier density may be determined. Additionally, depending on the carrier type (p or n) the hall voltage will be positive or negative which allows the carrier type of a semiconductor to be established.

The Hall Effect measurement system at LSBU is of bespoke design with discrete hardware, giving good measurement flexibility. Whilst the majority of the following hardware is commercially available; the configuration of the system was designed and assembled by the author.

The magnetic field is produced by an Oxford Instruments, water cooled, variable pole geometry electromagnet (Model N100), powered by a PC controlled power supply (Sorenson XG-100-15) capable of achieving a peak field strength of 1 Tesla (10,000 Gauss). A custom, solid state relay based, PC controlled switching unit was developed in-house by the author to permit automated pole reversal of the magnet. This was necessary as the power requirements of the magnet exceeded the capabilities of readily available switching solutions.

Current sourcing and monitoring and voltage measurement are provided by Keithley instruments hardware under PC control via GPIB. The Keithley measurement system consists of:

- A model 7065 Hall Effect matrix switching card, housed in a model 7001 switch mainframe, automating the multiple sourcing and measuring configurations applied to samples under test
- A model 6220 current source, capable of supplying currents in the range of 100 fA to 100 mA allowing for samples with wide resistivity ranges
- A model 2182A nano-voltmeter capable of measuring voltages in the range 1 nV to 100 V for high accuracy, low noise measurements of the induced Hall voltages in samples

Overall control of the various hardware components and data logging are handled by a bespoke software solution developed by Semimetrics Ltd. which allows for near complete automation of the measurement process once initial conditions are configured.

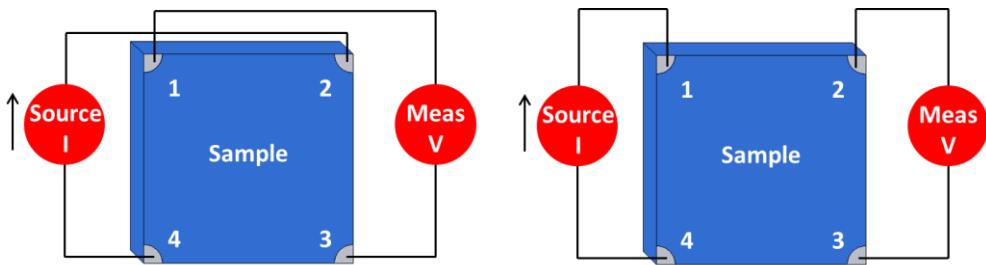


Fig 35. a) Resistivity measurement **b)** van der Pauw measurement

An important part of the Hall measurement process is the preparation and contacting of the sample where necessary. For optimal results, samples should be square, as near to uniform thickness as possible and with ohmic contacts if the sample is a semiconductor. To assess the uniformity of the sample prior to taking Hall measurements, the software runs a series of comparative resistance tests in the four combinations of current sourcing and voltage measurement (Fig 35a). If the sample is nominally uniform then the four values for resistance should be similar. Equally if the four contacts are ohmic, the four I-V plots should be linear and overlap. Clearly it is not always possible to achieve this ideal and the software is able to establish the level of non-uniformity and calculate a correction factor. Sensitivity testing of this capability was carried out by intentionally depositing non ideal contacts on identical samples and taking measurements. This investigation indicated that uniformity values not less than 0.7 (where 1 is perfect uniformity) are capable of being corrected successfully without substantially affecting the validity of the results.

Provided these requirements are satisfied, the Van der Pauw method (Fig 34b) is then applied to measure the sheet resistance and resistivity of the film. Then the process is repeated with a forward and reversed magnetic field applied to the sample to measure the Hall voltage. From this the doping type (p-type) or (n-type), sheet carrier density and carrier mobility may be calculated.

3.3.11. Ellipsometry

Ellipsometry is a multipurpose characterisation tool. It is a non-contact optical technique which can probe the dielectric properties of a thin film and establish the refractive index or dielectric function of the material. From this it is typically used as a means to characterise the thickness and composition of a film but can also be used to investigate crystallinity and to calculate doping concentration and conductivity of a sample.

Measurements are made by shining a polarised light source of known properties at the sample and measuring the change in polarisation of the reflected beam [227]. The polarisation state of the light shining upon the sample is defined by an *s* and *p* component

where the *s* component is oscillating perpendicular to the plane of incidence and parallel to the surface of the sample and the *p* component is oscillating parallel to the incident plane.

The ratio between the reflected *s* and *p* (r_s and r_p) is the complex reflectance ratio (ρ) of the sample and can be defined by two components; the amplitude ratio (ψ) and phase difference (Δ).

This gives the following equation:

$$\rho = \frac{r_p}{r_s} = \tan(\psi)e^{i\Delta} \quad (3.15)$$

As the measurement is a ratio rather than an absolute value it is resilient to effects like scattering from highly reflective samples and does not require standards or reference measurements to be taken. Conversely, because it is an indirect method and the optical constants of a sample cannot be directly calculated from the measured values the process relies on model analysis which is the primary potential source of error.

To calculate values for optical constant and layer thicknesses of a sample, a model of the layers must be produced. An iterative process is then carried out, varying optical constants of film layers and thickness parameters with values for ψ and Δ calculated using Fresnel equations [228]. The modelled values for ψ and Δ which best fit the measured values then provide the optical constants and thickness of film layers from the calculated values.

The aforementioned process assumes a monochromatic light source such as a laser and is referred to as single-wavelength ellipsometry. This permits the focusing of the beam to a very small spot size for location specific measurement but limits the setup to one set of ψ and Δ values. By utilising a broad band light source it becomes possible to probe the refractive index and dielectric function of a film across a range of wave lengths permitting more in depth material study than with a single wavelength. Ellipsometry carried out with a light output between the near infrared through to ultraviolet can be used to study the sub-band-gap region of films making analysis of features such as band-to-band transitions possible.

The system at LSBU is an Angstrom Sun technologies SE200BM with variable incident beam angle and a combination xenon and halogen light source allowing for analysis from 400-1000 nm. The system is PC controlled which runs software that operates the hardware and calculates various parameters based on the user defined model of the film being examined. Due to the bespoke nature of the hardware and software, it was not uncommon to experience glitches which required careful monitoring to ensure efficacy of data.

3.3.12. Junction Delineation by Grooving and Staining

Prior to the advent of secondary ion mass spectrometry or indeed when such a technique is not available, junction delineation by grooving and staining provides a means by which the depth of a diffused emitter may be ascertained [229].

The sample to be investigated first has a spherical groove ground into its surface by a rotating stainless steel ball coated with slurry consisting of fine (≈ 100 nm) diamonds suspended in a hydrocarbon paste. The groove must be of adequate depth to penetrate through the diffused emitter and into the substrate below exposing both parts of the junction. The sample is then thoroughly cleaned in toluene to remove residual diamond paste, rinsed in deionised water and dried in nitrogen.

The sample is then briefly dipped in a 1:1:2 ratio solution of hydrofluoric acid, chromium trioxide and deionised water. The chromium trioxide oxidises the surface of the silicon which is then etched by the hydrofluoric acid. However, p-type and n-type silicon etch at differing rates in the solution resulting in visibly contrasting regions in the two exposed areas. The difference may be observed using conventional visible light microscopy (Fig 36).

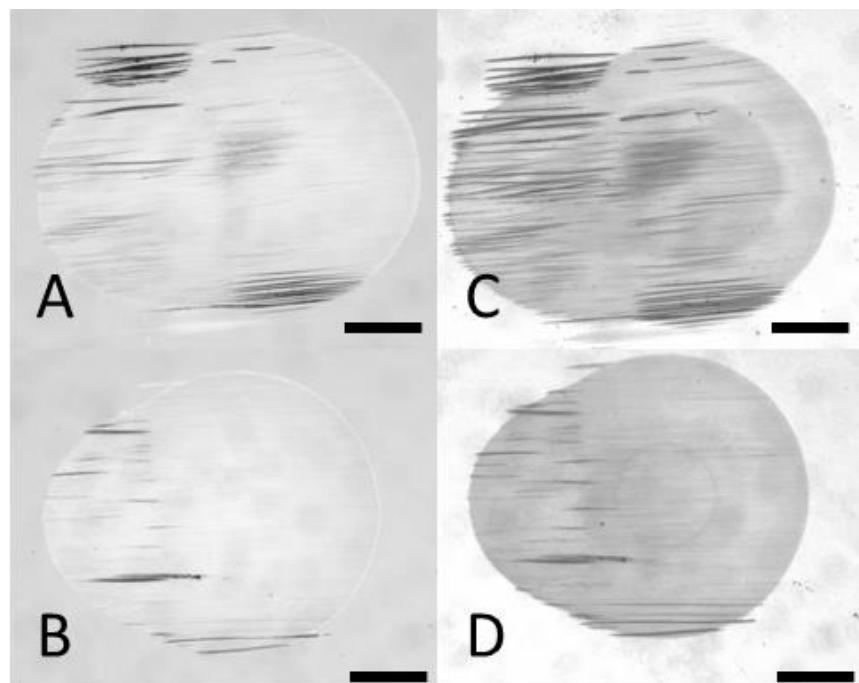


Fig 36. White light microscopy of ball grooved and stained silicon samples. A and B show the surface after grooving and C and D show the same samples after staining

By measuring the radii of the two differentiated regions, combined with the known radius of the steel ball, the junction depth is expressed by:

$$x_j = \frac{a^2 - b^2}{2R} \quad (3.16)$$

where x_j is the depth of the junction, R is the ball radius, a is the radius of the larger ring and b the radius of the smaller ring (Fig 37) [230][231]. Image analysis and measurements were made on images captured by a microscope mounted digital camera using the free analysis software ImageJ.

Due to the strictly visual nature by which the measurements are extracted from the microscope images and the fact that the edges of the different regions are not always clearly delineated the likely error for junction depth measurements is moderate. To this end, for samples where the edge of the delineated area was not cleanly defined, measurements were taken at the outer and inner limits of the visible edge. This variation then defined the error with which each junction depth was stated.

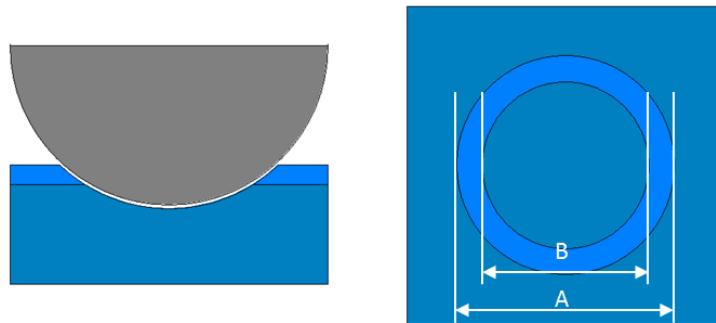


Fig 37. Junction delineation process diagram. Shown left is the ball bearing grooving the surface of a p-n junction device. Shown right are the dimensions extracted under white light microscopy that allows junction depth to be calculated

The system at LSBU is custom built and consists of a 50 mm stainless steel ball bearing driven by a variable speed controlled stepper motor. Samples are mounted on a vacuum chuck which is compressed against the ball bearing by an adjustable tension coupling to permit the grinding force to be varied. Various diameter diamond pastes (100 nm – 20 µm) were investigated as the grooving compound, however, pastes containing diamonds on the micron scale typically resulted in grooves with large scratches which resulted in difficulty discerning the junction with any accuracy. Ultimately the paste containing 100 nm diamonds was selected.

3.4. Conclusions

- This chapter has reviewed the various experimental and characterisation processes utilised throughout this project to fabricate and measure the parameters and performance of devices.
- A study of the theory behind solid state impurity diffusion has shown that it is possible to mathematically model the diffusion process and assess the likely junction position and doping concentration based on a set of initial parameters. However, the use of such models is more complex when rapid thermal processes are used as diffusion rates are known to be enhanced in the presence of growing oxides whose own growth rates are also affected by such processes
- A wide array of characterisation processes have been described to measure and analyse material and device parameters. Whilst many produce absolute results, others rely on fitting to models and it is important that these are appropriate to the situation or material to ensure meaningful results are obtained.
- The various deposition and processing tools used have been described. Particular challenges exist when using vacuum based deposition processes, especially with regard to accurately measuring temperature in a vacuum. Whilst absolute temperature may be difficult to establish, provided measurements are taken in a consistent fashion, repeatable results are generally achievable for equivalent temperatures.

Chapter 4. Device Fabrication Processes

This chapter will address the development of a variety of techniques required to produce complete, working solar cells including:

- Metal contacts fabricated by evaporation or sputter deposition for front and rear contacting of devices
- The application of a transparent conductive oxide (TCO) to act as a full area front surface contact
- The assessment of doped silicon layers prepared by chemical vapour deposition (CVD) as a means to fabricate an emitter on structure silicon
- The use of edge isolation to prevent emitter shunting and a number of means to achieve this

4.1. Rear Contacts

The rear contact of a solar cell serves two main functions. The first is to provide a low resistance ohmic contact to the substrate material, in this case p-type silicon wafer. The second is to act as a rear reflector to minimise through device transmission of incident light. This is not especially relevant for the devices that feature in this work as the substrate wafer is on the order of 675 μm thick, but would be an important consideration in thin film devices.

In almost all cases, metal contacts to p-type silicon are aluminium [232][233] as it is an abundant, cost effective material and can achieve low resistance and a good ohmic interface. It was deemed unnecessary to investigate alternative contacting methods due to the existing well documented method and instead experiments were undertaken to find the optimum means to implement this contacting technique using available processes.

Two methods to deposit aluminium were available; thermal evaporation and sputter deposition. Initial experiments were undertaken using the thermal evaporator and were intended to establish the necessary process conditions to achieve an ohmic response between aluminium films and the underlying silicon substrate.

Silicon wafer with resistivity 1-10 $\Omega \text{ cm}$ was cleaved into 25 mm^2 square samples which were cleaned in ultrasonically agitated acetone before being rinsed in deionised water and then blow dried in a stream of nitrogen (N_2). Subsequently they were placed in a piranha etch solution to remove organic contaminants before again being rinsed in deionised water and N_2 blow dried. The samples were then masked to produce two 4 mm^2 contact pads at 5 mm

spacing and loaded into the thermal evaporator. The evaporator was used to deposit 100 nm of 99.999% purity aluminium under high vacuum (1×10^{-6} mTorr) onto the masked samples.

After removal the samples were found to possess a level of resistance so high as to appear non-conductive. This is in agreement with literature, whereby the interface between the silicon and aluminium possesses non-ideal energy states which prevent an effective ohmic contact. Subsequently samples were subjected to a variety of different anneal processes to assess the ohmicity of the resulting contacts and their level of resistance (Fig 38).

The first anneal process investigated consisted of placing samples in a tube furnace at 500 °C for 60 minutes with an inert atmosphere of N₂. This was a previously established technique, known to produce an ohmic response and used as a reference for other processing methods. The other processes investigated were carried out in a rapid thermal annealing (RTA) system and consisted of various temperatures and cycle times.

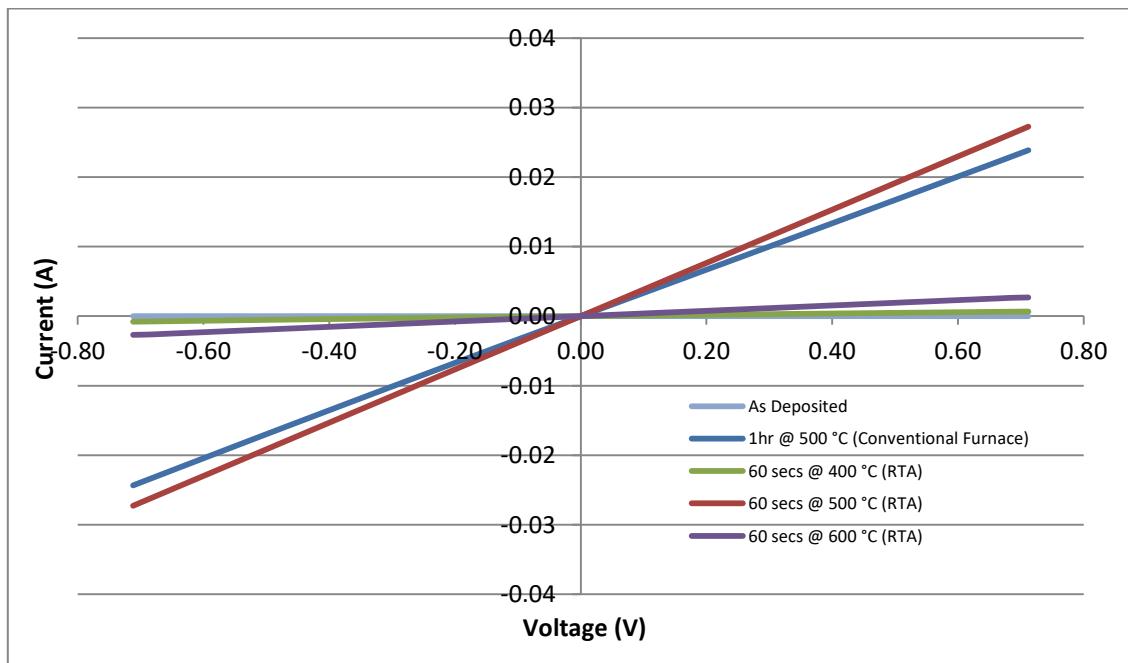


Fig 38. I-V data for different anneal processes on 100 nm thick Al contacts. Included are the as deposited contacts, the reference anneal undertaken in a conventional tube furnace and a variety of RTA annealing processes

All processing cycles investigated resulted in improvement over the un-annealed samples, however, the resistance of the contacts varied significantly. Samples annealed for 60 seconds at 400 °C were near ohmic with minor non-linearity in the negative voltage region; however, contact resistance was very high with through device resistances in the region of 48 kΩ. Samples annealed for 60 seconds at 500 °C were superior to the control samples with equivalent ohmicity and improved resistance. Samples annealed for 60

seconds at 600 °C demonstrated an equivalent level of ohmicity to samples annealed at 500°C but exhibited significantly higher through device resistance. The reasons for the varying contact performance are discussed in the following paragraphs.

At temperatures above approximately 350 °C a metallurgical interaction between the aluminium film and silicon substrate begins to occur. The aluminium film takes up silicon to the limit of solubility at the given temperature (up to $\approx 1\%$ at 550 °C). When the sample is cooled the dissolved silicon is rejected and recrystallizes at the interface but is now heavily p-type doped by the aluminium with concentrations $\geq 1 \times 10^{19}$ atoms/cm³ observed [233]. As no liquid phase is formed but interaction takes place this process referred to as solid phase epitaxy. This heavily doped p-type region results in a narrow, fully depleted depletion region at the metal/semiconductor interface with reduced barrier height. This reduction in barrier height creates a situation where electrons are able to tunnel across the junction [234].

Above 577 °C a change takes place in the anneal process as at this temperature silicon and aluminium form a eutectic phase (see Fig 39) with an aluminium-silicon melt forming at the material's interface. The amount of silicon dissolved in the aluminium melt is dictated by the temperature attained during the annealing process. Upon cooling silicon is rejected from the aluminium melt until the eutectic concentration of 12.2% is reached. The melt recrystallizes epitaxially at the interface between the silicon and the melt, incorporating the aluminium as a dopant and resulting in a shallow, highly doped p-type region. This type of contact is generally referred to as an aluminium back surface field (BSF) [235].

There are two proposed explanations for the inferior performance of the contact annealed for 60 seconds at 600°C. The first relates to the cooling rate of the sample following the peak temperature. At the end of the anneal step the temperature is allowed to fall at the maximum rate the system can cool naturally which equates to approximately 25 °C/s. As a result the temperature falls from above the eutectic melt temperature to below in approximately 1 second. This rapid cooling rate is likely to result in poor quality recrystallization of the silicon melt at the metal semiconductor interface.

An alternative explanation relates to the thin contact layer of aluminium deposited (≈ 100 nm). It is possible that the entire aluminium thin film becomes saturated with silicon whereupon cooling the entire layer is effectively replaced with a highly doped p-type silicon region with no remaining metal region to act as a contacting point. This silicon, whilst highly doped, would possess a higher resistance than the previously present aluminium layer resulting in the poor conductivity. Visual examination would seem to lend credence to this as the post deposited film took on a blueish hue suggesting that the film had been entirely converted into a highly doped silicon/aluminium layer.

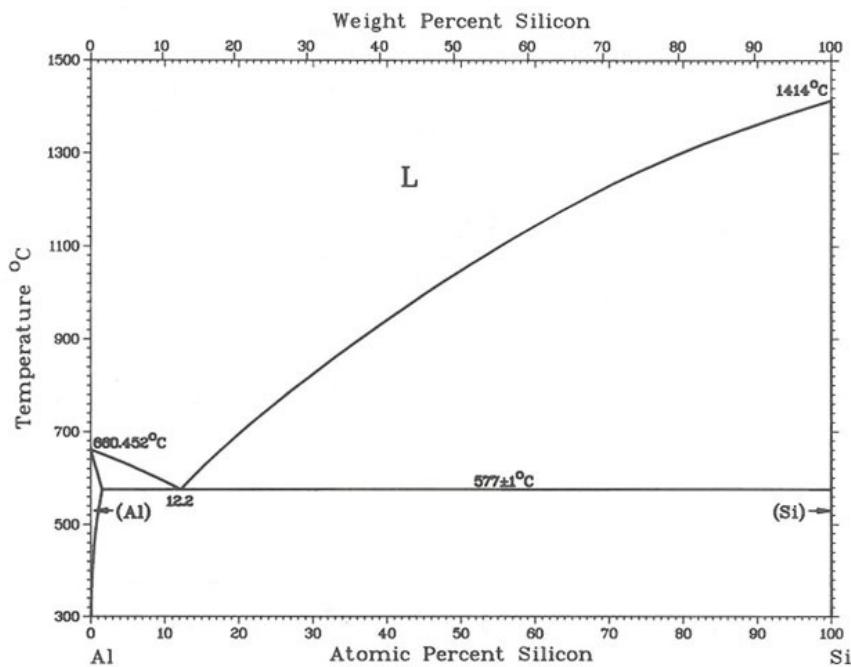


Fig 39. Aluminium-Silicon phase diagram [236]

Commercial solar cells typically utilise rear contacts with thicknesses on the order of 20 µm to minimise the sheet resistance of the contact film. Through the use of screen printed metal pastes it is trivial to achieve films of this thickness. A paste based metallisation process was unavailable for this work, however, so it was not possible to achieve thicker contacts than investigated to this point via this method.

Whilst theoretically it would be possible to attain thicker contacts using thermal evaporation there were two limitations preventing this approach. The first was a physical limitation on the quantity of source aluminium that could be held within the tungsten baskets used to heat the material. It was found that 300 nm – 400 nm was the maximum achievable film thickness with the available source material. The second limitation was the thermal load applied to the substrate and deposited film by being in proximity to a tungsten basket heated to in excess of 800 °C. It was postulated that extended periods of proximity to the heat source could result in a level of annealing of the contacts during the evaporation process with the associated modification of their properties.

Sputter deposition offered a viable alternative to depositing the required aluminium film with neither of the limitations inherent to the thermal evaporation process. It was possible to achieve a rear contact thickness of 1.5 µm utilising the process conditions listed in Table 2.

Source Target	Aluminium
Power Set Point (W)	350 W
Process Pressure (Torr)	15 mTorr
Ar Flow Rate	25 sccm
Sputter Period	120 minutes

Table 2. Sputter process conditions for the application of experimental aluminium rear contacts to p-type silicon.

If one considers the equation for sheet resistance of a thin film [237]:

$$R_{sh} = \frac{\rho}{t} \quad (4.1)$$

Where R_{sh} is the sheet resistance in ohms/square (Ω/\square), ρ is the bulk resistivity in ohm cm ($\Omega \text{ cm}$) and t is film thickness in cm. Taking the bulk resistivity value for aluminium as $2.82 \times 10^{-10} \Omega \text{ cm}$, the sheet resistance of the aluminium contact falls from $2.82 \times 10^{-5} \Omega/\square$ for a 100 nm thick contact to $1.88 \times 10^{-6} \Omega/\square$ for the 1500 nm thick contact.

Whilst this improvement in sheet resistance of the contact layer itself is beneficial for collection of current over the rear surface, it does not consider the resistance between the metal and semiconductor itself. To assess this it is necessary to apply the transfer line method (TLM). This involves taking resistance measurements between pairs of contacts deposited on the surface of the semiconductor at varying distances then plotting these resistances against the distance between pairs. It is possible to extract from the resulting plot the contact resistance R_c in ohms (Ω) and from this the contact resistivity ρ_c in ohms cm^2 ($\Omega \text{ cm}^2$).

Fig 40 contains the plotted TLM data for a series of $1.5 \mu\text{m}$ thick contact pads with spacing values that increase by a factor of two annealed for 30 mins at 500°C . The y-intercept value is equivalent to twice the contact resistance ($2R_c$) giving a value for R_c of $0.28 \pm 1.5 \times 10^{-3} \Omega$. From this a value for contact resistivity can be calculated by multiplying the contact resistance and the contact area, giving a value of $3.3 \times 10^{-2} \pm 1.8 \times 10^{-4} \Omega \text{ cm}^2$.

This is using the simplified TLM method as described in section 3.3.9. Taking into account the current crowding also described in the aforementioned section, an adjusted value for contact resistivity of $2.62 \times 10^{-2} \pm 1.47 \times 10^{-3} \Omega \text{ cm}^2$ is found.

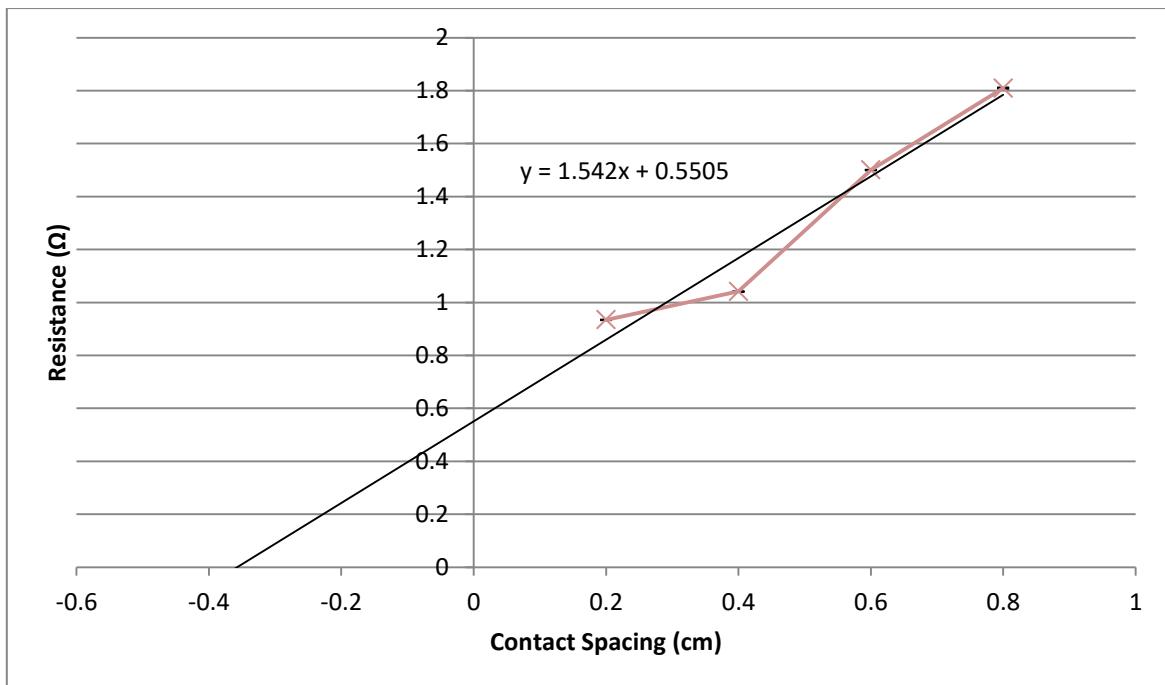


Fig 40. Application of the transfer line method. The resistance values for each contact spacing are plotted and the trend line extended back to the y-axis, with the intercept being twice the contact resistance.

The same contacting arrangement was annealed using the RTP method of 60 seconds at 500 °C and the TLM method used to assess the resulting contact resistance. A reduction to $7.11 \times 10^{-3} \Omega \text{ cm}^2$ was observed for contacts annealed in this way. It is proposed that the short anneal cycle achieves the necessary solid phase epitaxy to produce an ohmic contact whilst ensuring that the highly doped p-type region underneath the contact is kept shallow and adequate aluminium is retained for a metal contact pad. Whilst the p+ region is highly conductive it is still comparatively resistive when compared to the metal contact itself and if unnecessarily thick will add to the resistance path.

4.2. Front Contacts

The front side of fabricated devices consists of an n-type emitter, which requires a different approach to contacting than that employed for the rear side p-type contact. Whilst aluminium provides both a convenient metal choice and a p-type dopant to create a p+ region, no convenient and/or non-toxic equivalent metal exists for n-type contacting.

A common alternative means to contact n-type silicon is the use of metals which form a silicide. There are a number of possible choices used in silicon silicide formation including titanium, cobalt, nickel, palladium, platinum and tungsten. Of the aforementioned metals,

three are immediately challenging; tungsten is difficult to deposit due to its high melting point, platinum is prohibitively expensive and cobalt has some toxic properties.

Palladium has been demonstrated to form a useful silicide contact to silicon [238][239] but is in the same family as platinum and whilst slightly cheaper it is still an expensive choice of metal with poor scalability. Titanium is straightforwardly deposited by sputtering and significant research has been undertaken into its use as a contact to silicon [240][241][242]. It has been shown; however, that the formation of both titanium-silicide phases (C49 & C54) is retarded in the presence of heavily phosphorus doped silicon [243][244]. The result is shallow silicide regions which demonstrate increased contact resistance. As the emitter layers for the micro-pillar devices under investigation must necessarily be highly doped, this makes titanium a potentially problematic choice.

The remaining metal choice, nickel, does not demonstrate any silicide formation issues related to material doping concentration [245] making it a suitable choice for the highly doped, shallow emitters to be employed in this work. As most silicide contacts rely on a thin layer of the silicide forming metal with a thicker metal pad deposited atop them, it is important that during thermal processing the formed metal silicide and the cap layer do not interact with one another to form undesired alloys. Whilst titanium silicide is reportedly stable to a temperature of about 480 °C [246], nickel has demonstrated stability up to 700 °C [247] adding the potential advantage of a wider processing temperature range for other process steps.

4.2.1. Ni/Ag Contacts

Nickel was selected for further investigation as it can be easily deposited by thermal evaporation and is abundant making it a practical real world choice. Like the majority of other silicide forming metals, nickel forms multiple phases with silicon of which NiSi is the preferred phase with low resistivity [248]. As nickel reacts with air when heated, it was necessary to apply a capping layer to protect it during the post deposition anneal cycle. Aluminium would be a suitable choice, however, from previous experimental work it was noted that aluminium heavily wets the tungsten baskets used for material heating in the thermal evaporator. This wetting meant baskets were only suitable for single use making an alternative choice preferable. It was found that silver does not wet the tungsten baskets allowing for multiple depositions. Silver is highly conductive and was known not to react under the processing conditions required for NiSi formation making it a suitable choice. Copper was considered as an alternative to silver for the cap layer; however, it has a very high diffusivity in silicon and causes deep-level defects. As the sputter system that would be

required for copper deposition was also used to apply rear contacts and TCO layers, the risk of contamination and associated device performance degradation was deemed unacceptable.

A heavily doped n+ silicon wafer with $0.001 \Omega \text{ cm}$ resistivity was selected to act as a model for the n-type emitter, this removed any variation in doping concentration from the analysis of the contacting and permitted direct comparison between the different configurations. The samples were masked to deposit two 2 mm dot contacts at 5 mm spacing. A thickness of 15 nm for the Ni layer was selected for the nickel layer to provide adequate thickness for silicide formation without creating unnecessary resistance in the contact path. This was then capped with 1 μm of silver to protect the nickel during annealing and thicken the contact.

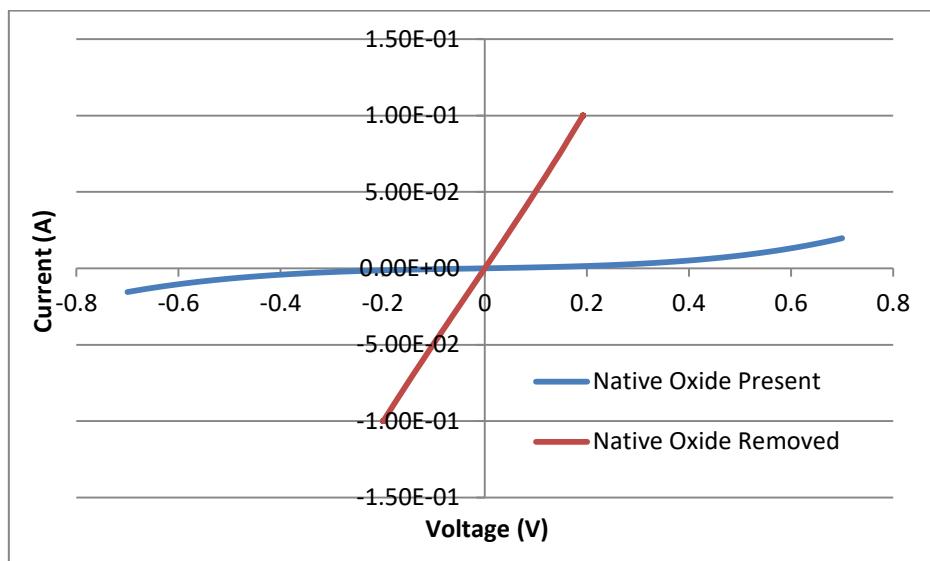


Fig 41. Current voltage plots for Ni/Ag contacts on n-type silicon with and without the native oxide

Investigation of literature suggested a suitable annealing temperature in the $300 \text{ }^\circ\text{C}$ range. Despite the aforementioned stability of nickel silicide it was decided not to anneal at temperatures exceeding $400 \text{ }^\circ\text{C}$ to minimise any chance of undesired interactions between the silicide and the metal layers occurring. Within these limits, a variety of anneal times and temperatures were investigated to locate the optimum parameters.

It was found that removal of the native silicon oxide prior to the deposition of the metal contact layers was crucial to the formation of a low resistance contact. Contacts deposited with the native oxide in situ were on average an order of magnitude more resistive as well as being non-ohmic (see Fig 41). It was not expected for this to be the case for nickel [249] and the reason for the sensitivity to interfacial oxides of this particular contacting regime is unclear.

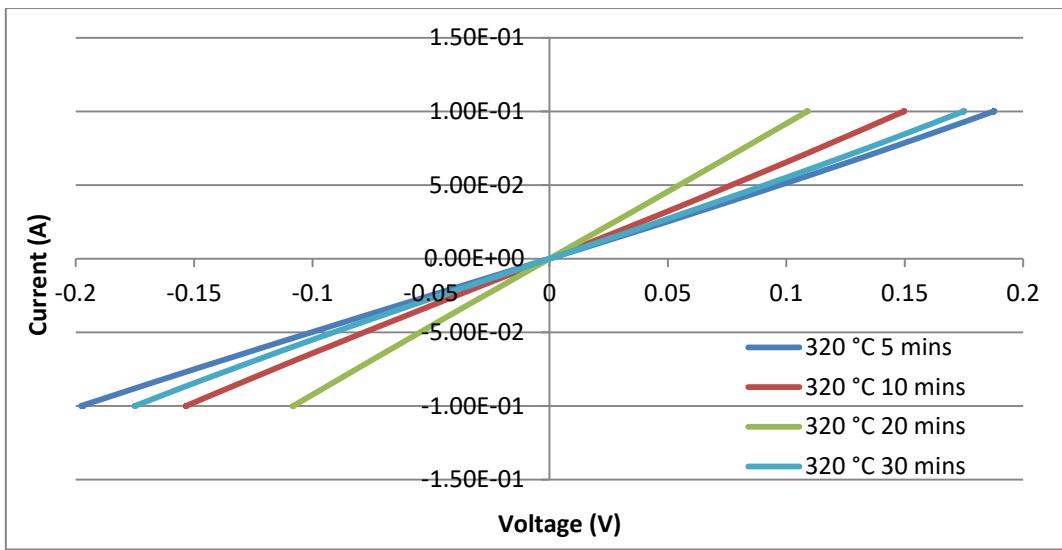


Fig 42. Current voltage plots for Ni/Ag contacts on n-type silicon for various annealing times at 320 °C

The first series of samples were annealed at 320 °C for various times (see Fig 42). The ideal scenario is near complete consumption of the nickel layer into the nickel silicide interface with the silver contact pad sat directly atop it. However, whilst silver can be used as a contact to n-type silicon, under non-optimal conditions a Schottky contact may be formed which is clearly undesirable. It was important therefore that the anneal period was adequate but not longer than necessary.

A steady improvement in through-contact resistance is observed with increasing anneal time up to 20 minutes at which point the subsequent anneal at 30 minutes yields a significant drop off. The I-V plot indicates the contact is still ohmic which indicates that no detrimental interaction between the silicon and the silver cap layer has taken place and the exact cause of the rise in resistance is unknown.

Subsequently, a fixed time of 10 minutes for annealing was selected and the temperature varied to assess the effect on the resulting contacts (see Fig 43). Whilst annealing at 350 °C demonstrated an improvement over the 320 °C anneal, further increasing the anneal temperature to 400 °C resulted in a rise in resistance although still an improvement over the 320 °C process. It should be noted, however, that the 350 °C for 10 minutes anneal resulted in a near identical resistance to the 320 °C for 20 minute anneal from the previous experiment series. Despite variation in the contact resistance for the various anneal temperatures and periods, all processes demonstrated ohmic contacts confirming the resilience of the nickel interface layer to inter-diffusion and non-ideal interactions suggested by literature.

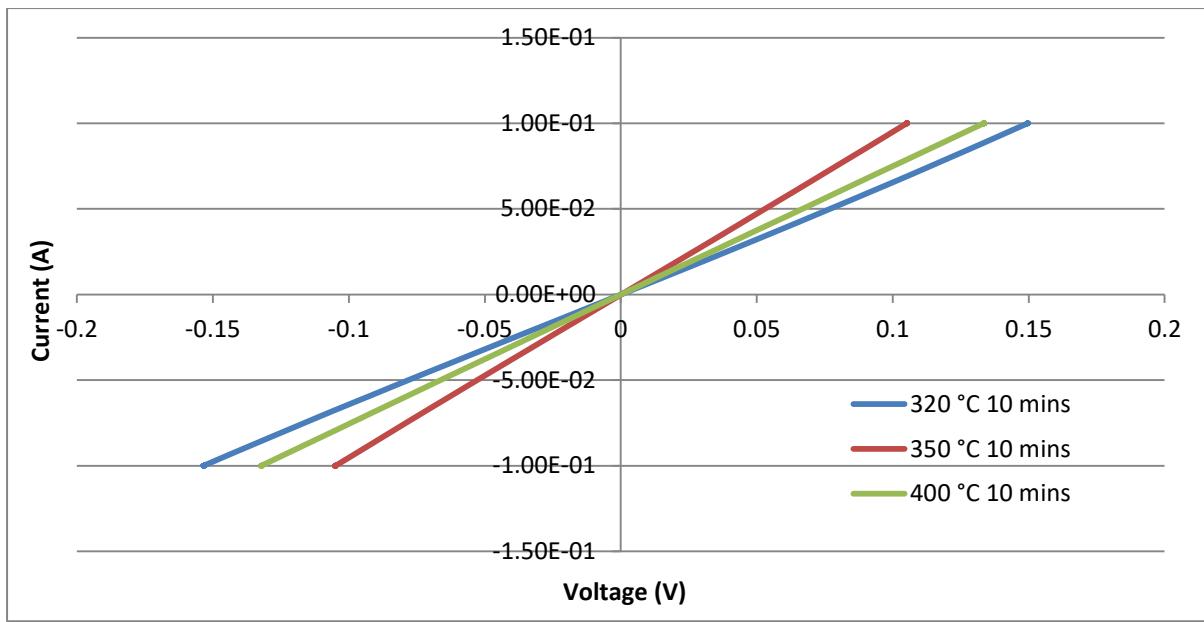


Fig 43. Current voltage plots for Ni/Ag contacts on n-type silicon at different annealing temperatures for 10 minutes

4.3. Development and Optimisation of AZO TCO Layers

To facilitate the contacting of structured solar cell samples, development of a transparent conductive oxide (TCO) was undertaken.

Indium tin oxide (ITO) is commonly used for this purpose, however, for a variety of reasons it was decided not employ this approach. The first was related to deposition temperature, which must typically be in excess of 400 °C to obtain the lowest achievable sheet resistance values for ITO [250]. Due to thermal coupling issues between the heater and sample stage of the sputter system at LSBU, it was difficult to achieve sample temperatures in excess of 300 °C which would have limited the performance of ITO layers. The second is the added complexity of having to reactively sputter metallic indium-tin targets with oxygen to produce the ITO and the associated potential for variation of film stoichiometry from run to run. Whilst sputtering from powdered oxide based targets has shown some success, the as deposited films are generally inferior to reactively sputtered films and require high temperature (>700 °C) annealing to attain the best achievable values [251]. A final limitation is the effect that post deposition annealing has on optimised ITO films, which whilst not required for the ITO itself, may be necessary for other device processing steps. When annealed in air, ITO films absorb oxygen, and the number of available oxygen vacancies is reduced. These vacancies are responsible for the films conductivity and resultantly it will fall. [252]. It is possible that annealing in a high vacuum might negate this process, but this increases the complexity of device processing and in addition was not a capability possessed by LSBU.

Zinc oxide (ZnO) in various forms is seeing increasing use as a TCO due to its lower cost, use of abundant materials and relatively low deposition temperature requirements compared to indium tin oxide (ITO) [253]. ZnO in its native state demonstrates weak n-type doping with associated high resistivity [254]. Various causes for this native doping have been proposed, including native defects [255] and inclusion of hydrogen [256] amongst others. The addition of a small percentage of aluminium changes its properties from resistive to highly conductive whilst retaining good optical transmission properties [257], making aluminium doped zinc oxide (AZO) a convenient choice for the purposes of this work. Furthermore, AZO can be deposited effectively by sputtering from a compound target, adding to its advantages as a TCO. Additionally, it is shown in literature [258], that AZO deposited at low sputter power (<150 W) suffers a similar fall in conductivity to ITO when annealed post deposition. However, it has also been found that AZO deposited at higher sputter power (>200 W) is less effected by post deposition annealing [259] and is believed to be due to the replacement of thermally sensitive intrinsic oxygen vacancies with thermally stable extrinsic aluminium dopant. This potentially makes AZO more suitable as a TCO when thermal processing steps are required during device fabrication.

Whilst the properties of AZO have been extensively studied, it was necessary to establish the optimal configuration of the hardware at LSBU to attain the performance levels which are known to be achievable. For an AZO film on glass this typically equates to a resistivity in the mid $1 \times 10^{-4} \Omega \text{ cm}$ range and a transmittance of 80-85% [260].

To this end, multiple sputter runs were carried out using LSBU's JLS MPS sputter system loaded with a AZO (98% ZnO:2% Al) target and Corning 1737 glass as the substrate material. Prior to deposition, the glass was cut into 25 mm^2 samples which were initially cleaned in acetone in an ultrasonic bath, followed by a deionised water rinse and nitrogen blow dry. They were then subjected to a piranha etch and additional rinse and dry steps.

Substrate temperature, sputter power and chamber pressure were varied and all depositions were carried out for 30 minutes with a 5 minute pre sputter period at 100 W RF power to condition the target and remove any residual impurities. The process gas was 20 sccm of argon flowed through the chamber; sample height was fixed for all runs and samples were rotated at 20 rpm. All temperatures are as measured at the surface of a control sample. Due to the poor coupling of heat sources to samples in a vacuum it was necessary to run at set temperatures in excess of 600 °C to achieve measured temperatures between 150-300 °C.

The electronic performance of the films was characterised by four point probe and Hall Effect measurements whilst optical properties were examined using spectrophotometry. To permit straightforward comparison of the transmittance of the deposited films, in addition to the full

spectra, integration under the curve was used to calculate the area under each curve. This area was then normalised to the transmittance of Corning 1737 glass giving transmittance as a percentage of that of an uncoated glass sample.

4.3.1. Effect of Substrate Temperature on AZO

Whilst the surface temperature of the substrate does not directly affect the sputtering component of the deposition process, it affects the properties of the deposited film. Aluminium zinc oxide has a crystalline structure and its formation changes its performance, especially in the electrical domain. Increasing the surface temperature promotes growth of larger grains and resultantly fewer grain boundaries exist to hinder electron transport across the surface. Additionally, the greater energy available with increased surface temperature permits the diffusion of the Al dopant component to the surface of the film, further improving its carrier transport properties [261].

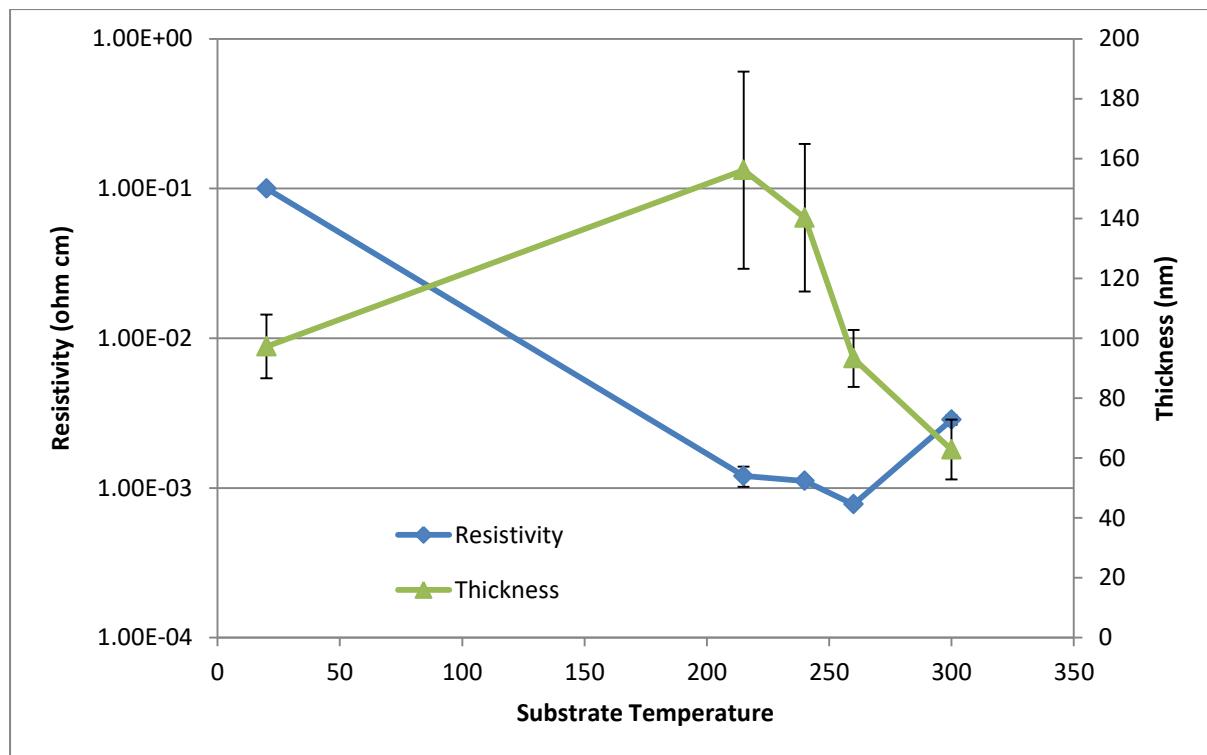


Fig 44. Effect of Substrate Temperature on AZO Thickness and Resistivity

Fig 44 shows the effect of varying substrate temperature on the resistivity of deposited AZO films. For all substrate deposition temperatures investigated there was a substantial improvement in resistivity over the film deposited at ambient temperature ($\approx 20^\circ\text{C}$). This is predominantly due to increased level of aluminium dopant that is taken up by the film in agreement with literature [262]. Furthermore, the increase in resistivity above 260°C is also in agreement with literature. It has been proposed that this is due to excess aluminium

uptake with increasing surface temperature resulting in the creation of scattering sites at grain boundaries which reduce film conductivity [263].

The reduction in film thickness with increasing temperature runs contrary to what might be expected as sputtered film thickness is generally a function of sputter time. However, this variation has been noted in literature [264] and is believed to be dependent on the sticking co-efficient of a material, which is a function of surface temperature [265].

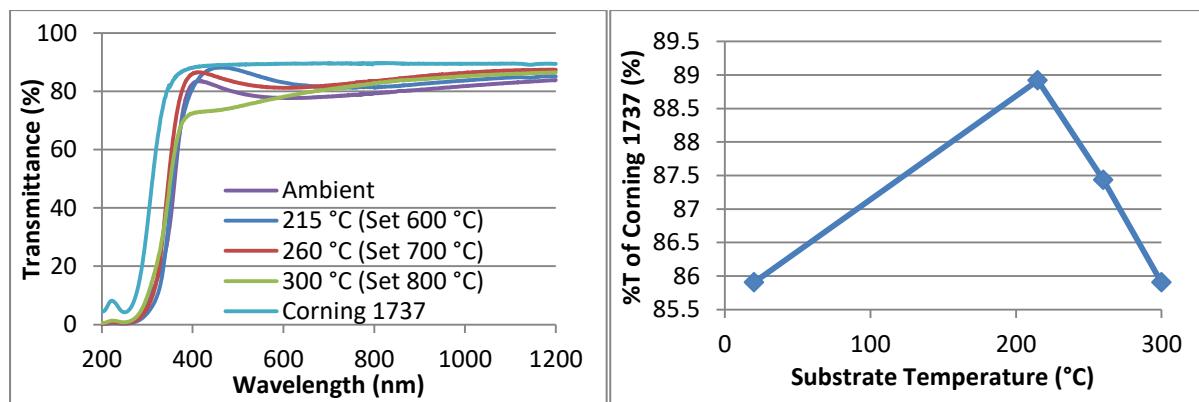


Fig 45. (a) Effect of substrate temperature on AZO transmittance and **(b)** AZO transmittance relative to Corning 1737 control

Fig 45(a) shows the transmittance spectra for the AZO films deposited at the various temperatures and an uncoated piece of Corning 1737 for comparison. Above 1200 nm the transmittance begins to fall as the IR wavelengths are absorbed through oscillations of free electrons in the conduction band. Fig 45(b) shows total transmittance of each sample as a percentage of uncoated glass. It is apparent that AZO deposited at ambient temperature has a lower transmittance compared to that deposited with temperature but based on the available data it is not possible to establish where the maximal point lies. What can be inferred is that the best optical properties and best electronic properties are achieved at different deposition temperatures with a resultant compromise required. Conveniently, the loss in equivalent transmittance is only 1.5% from the peak optical performance at 210 °C to the peak electronic performance at 260 °C which is a reasonable compromise.

Figure 46 shows the effect of substrate surface temperature on the morphology of deposited films by way of AFM imaging. The main effect is on the feature size or roughness of the crystalline film with a clearly visible increase in feature size between the ambient deposited film and that prepared at 260 °C. It is not clear if each feature or “lump” reflects an individual grain or collections of smaller grains, however, an increase in deposition temperature has been observed to promote grain growth [266]. The increase in surface roughness with raised

deposition temperature could account for the increased transmission as rough films tend to exhibit lower reflection.

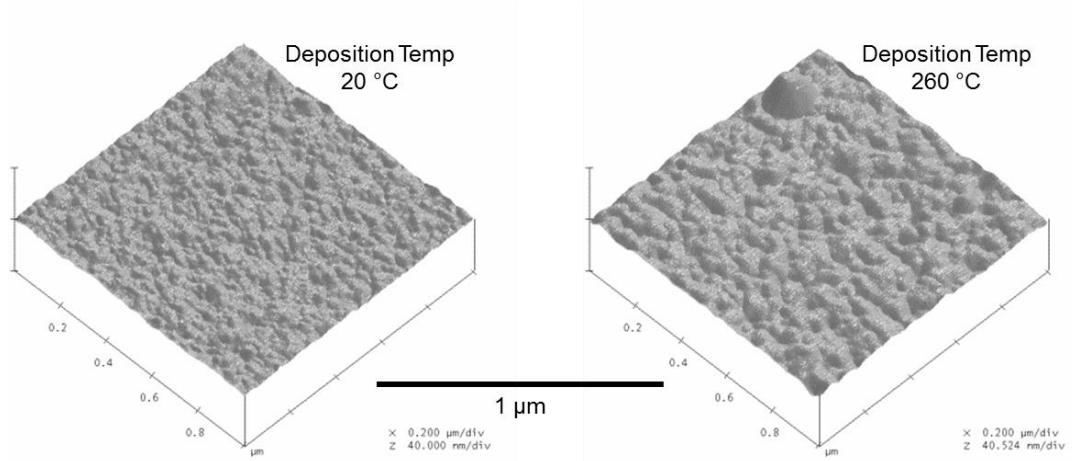


Fig 46. AFM images of AZO films deposited at ambient ($20\text{ }^{\circ}\text{C}$) and at the optimum electronic temperature of $260\text{ }^{\circ}\text{C}$, demonstrating the increased surface roughness with elevated deposition temperature

4.3.2. Effect of Pressure on AZO

The variation of chamber pressure can have a significant effect on the sputtering process as it directly affects the plasma density. Whilst adequate plasma density is important to ensure efficient sputtering of the target, excessively dense plasma can result in a large number of scattering collisions which limit substrate deposition.

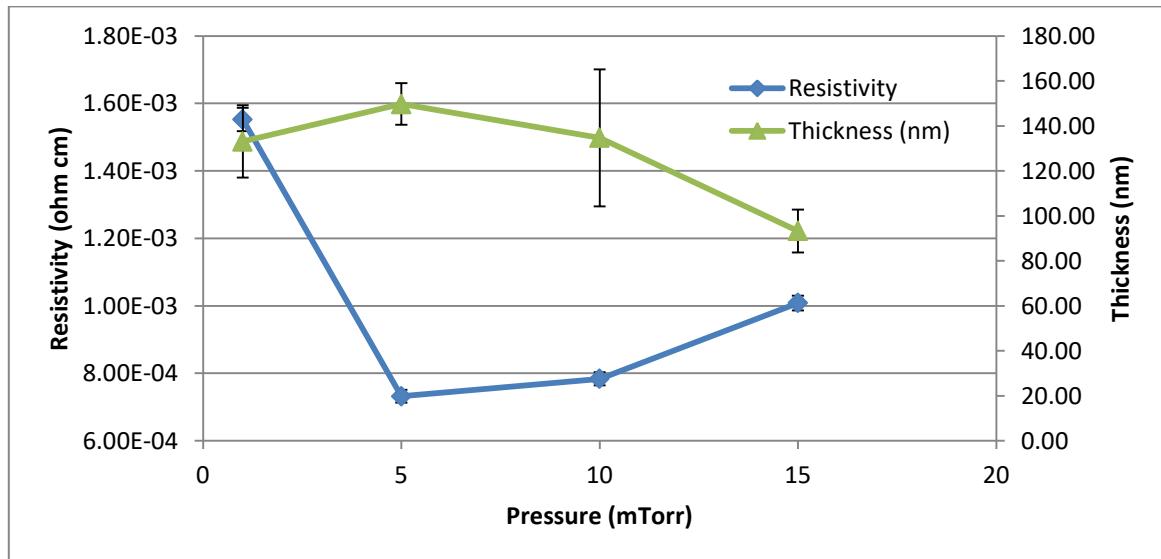


Fig 47. Effect of Process Pressure on AZO Thickness and Resistivity

Fig 47 shows the effect of varying process pressure on the resistivity and thickness of AZO films deposited at a process temperature of 260 °C and 100 W sputter RF power. The thickness increases steadily with decreasing pressure until a maxima point at 5 mTorr. Further reduction in pressure to 1 mTorr leads to a slight fall in film thickness but a substantial increase in resistivity. This resistivity value is far greater than that exhibited by the film deposited at 10 mTorr despite both films possessing broadly comparable thickness. This reason for this can be explained by examining the Hall Effect data for these points (Fig 48) which highlights a fall in carrier concentration for the 1 mTorr deposition. It is of course also the case that the 5 mTorr deposition exhibits a lower carrier concentration than that at 10 mTorr, yet exhibits superior resistivity. In this case, the lower carrier concentration is offset by greater carrier mobility.

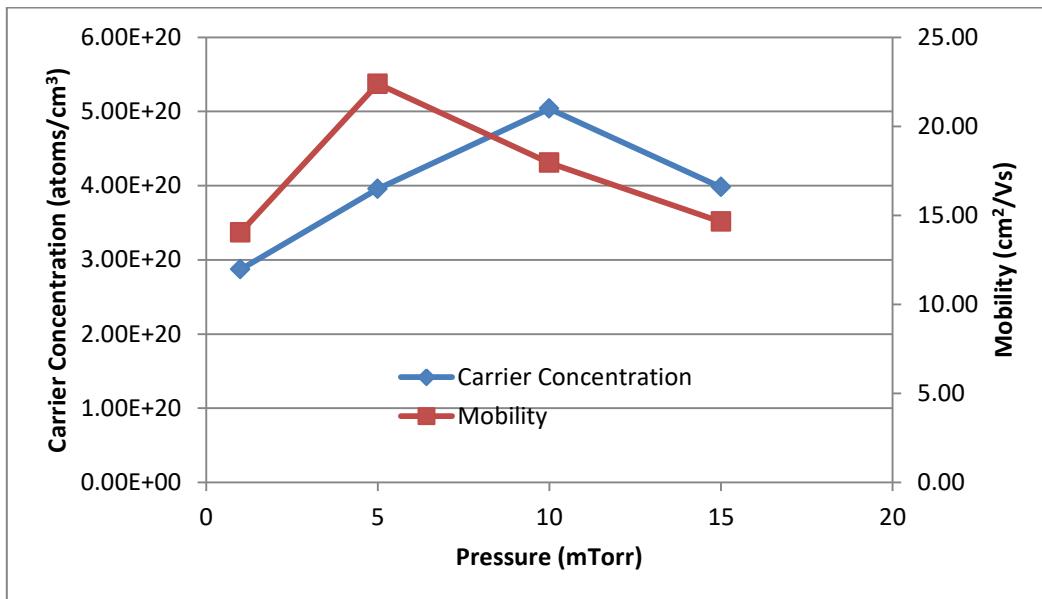


Fig 48. Effect of process pressure on carrier concentration and mobility

Fig 49(a) shows the transmittance spectra for the AZO films deposited at the various process pressures and an uncoated piece of Corning 1737 for comparison. Fig 49(b) shows total transmittance of each sample as a percentage of uncoated glass. From Fig 49(b) it can be observed that a fall in process pressure results in a fall in transmittance, however, from Fig 47 it can be observed that falling pressure also results in a thicker film. It is possible therefore that the change in transmittance simply results from the changing thickness of the deposited film in agreement with observations in literature [267].

An alternative theory can be put forward by observing the AFM and SEM data in Fig 50. It is evident that reducing the process pressure results in reduced surface roughness of the films with a resultant loss in scattering. The increasingly smooth films may therefore possess a

higher level of reflectance which would account for some of the loss in transmittance with reduced pressure.

It is likely that the result is actually a combination of the two aforementioned effects to one degree or another.

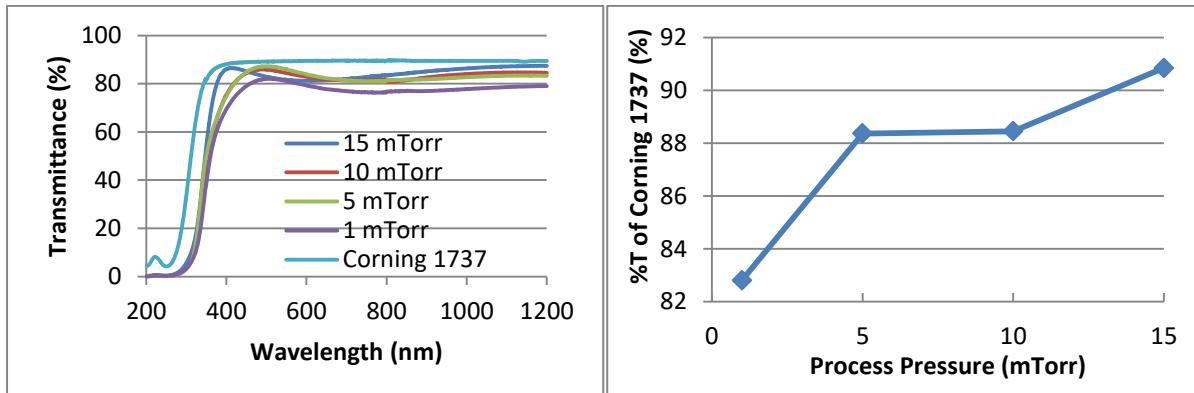


Fig 49. (a) Effect of Process Pressure on Transmittance and **(b)** Transmittance Relative to Corning 1737 Control

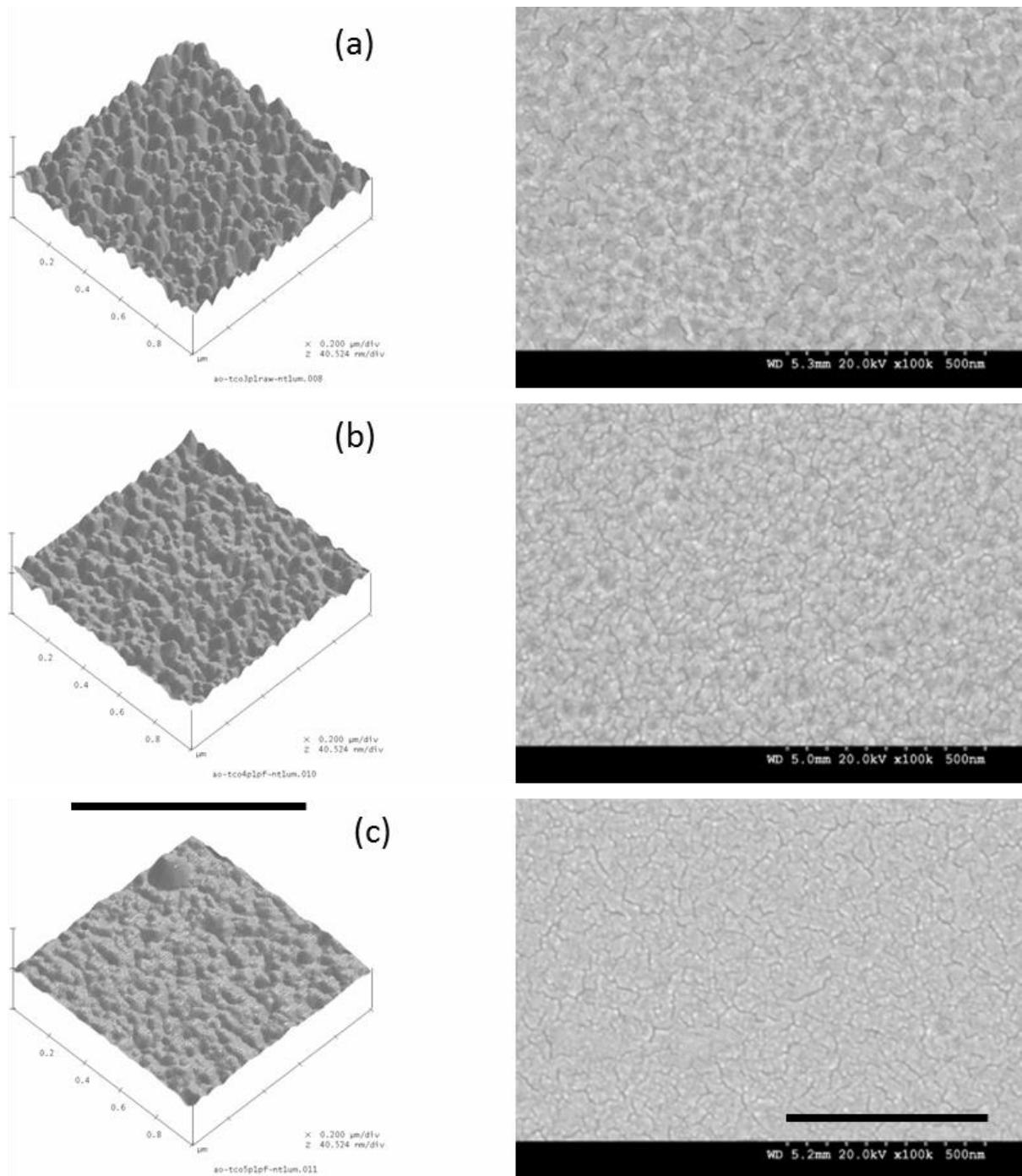


Fig 50. AFM and SEM images of AZO films deposited at various process pressures. Sample (a) was deposited at 15 mTorr, (b) was deposited at 10 mTorr and (c) was deposited at 5 mTorr. It can be observed that surface roughness progressively falls with reducing process pressure. Scale bars are shown in black with AFM scale representing 1 μm and SEM scale representing 500 nm.

4.3.3. Effect of deposition power on AZO

The primary effect of deposition power on the sputter process is the energy imparted to the ions in the plasma.

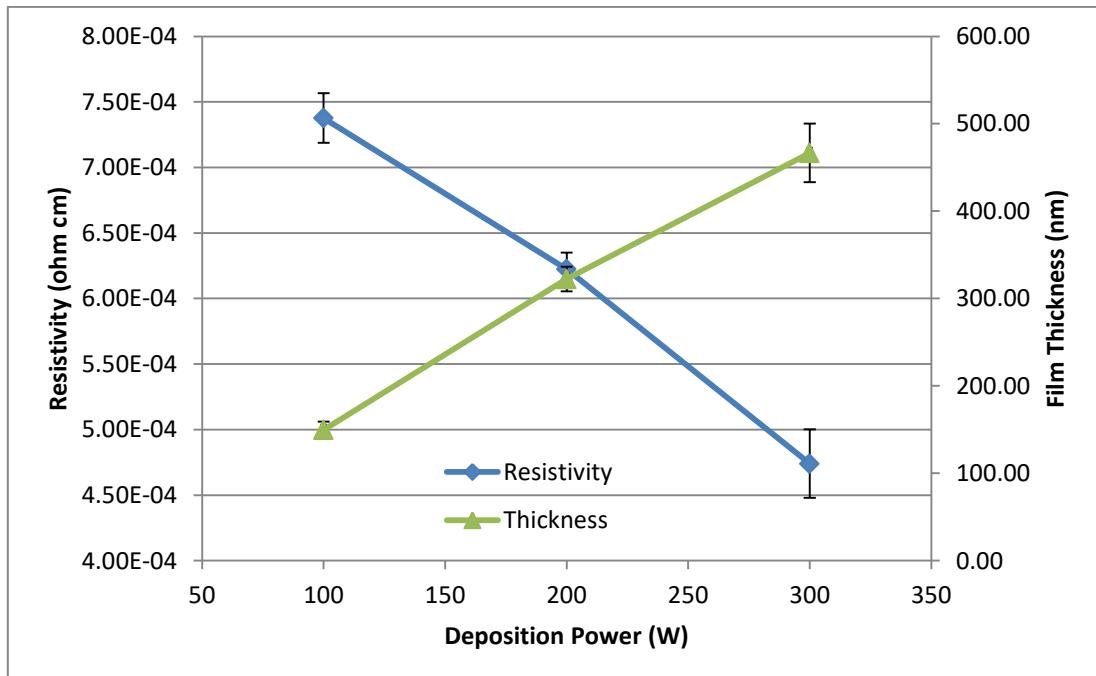


Fig 51. Effect of Deposition Power on AZO Thickness and Resistivity

Fig 51 shows the effect of deposition power on the thickness and resistivity of AZO films. As expected an increase in deposition power results in a thicker film with a broadly linear relationship between power and thickness. The improvement in resistivity with increasing power is believed to be due to better crystallinity of the deposited film and an enhancement of substitutional aluminium doping with greater deposition energy [268].

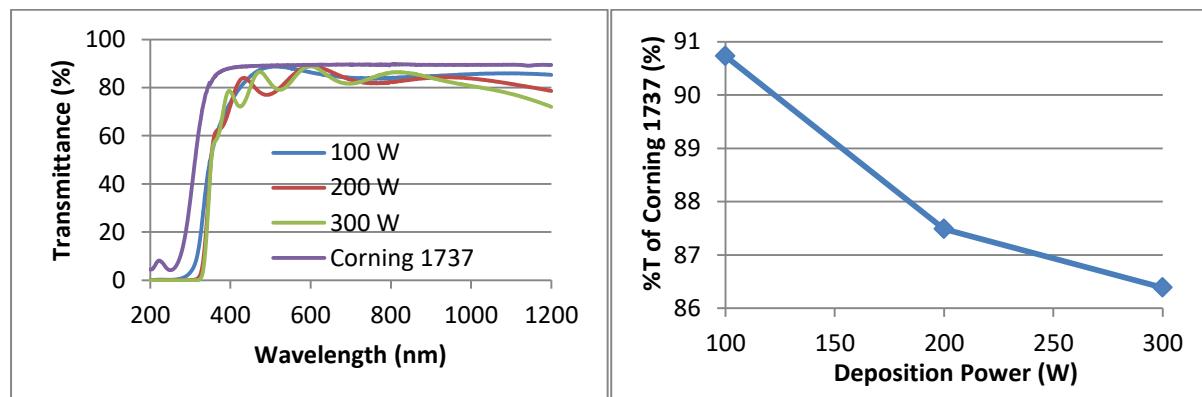


Fig 52. (a) Effect of Deposition Power on Transmittance and **(b)** Transmittance Relative to Corning 1737 Control

Fig 52(a) shows the transmittance spectra for the AZO films deposited at various deposition power levels and an uncoated piece of Corning 1737 for comparison. Fig 52(b) shows total transmittance of each sample as a percentage of uncoated glass. From the data it can be observed that an increase in deposition power results in a fall in total transmittance. As the film thickness increases quite substantially with increasing power this result is largely to be expected. Of note is the increase in oscillation in the full wavelength spectra with increasing deposition power. AZO is known to possess anti-reflective properties and these properties are dependent on film thickness. By modelling the reflection of the different thickness of the AZO films on glass (Fig 53) it is possible to identify the cause of the oscillation in the transmission spectra.

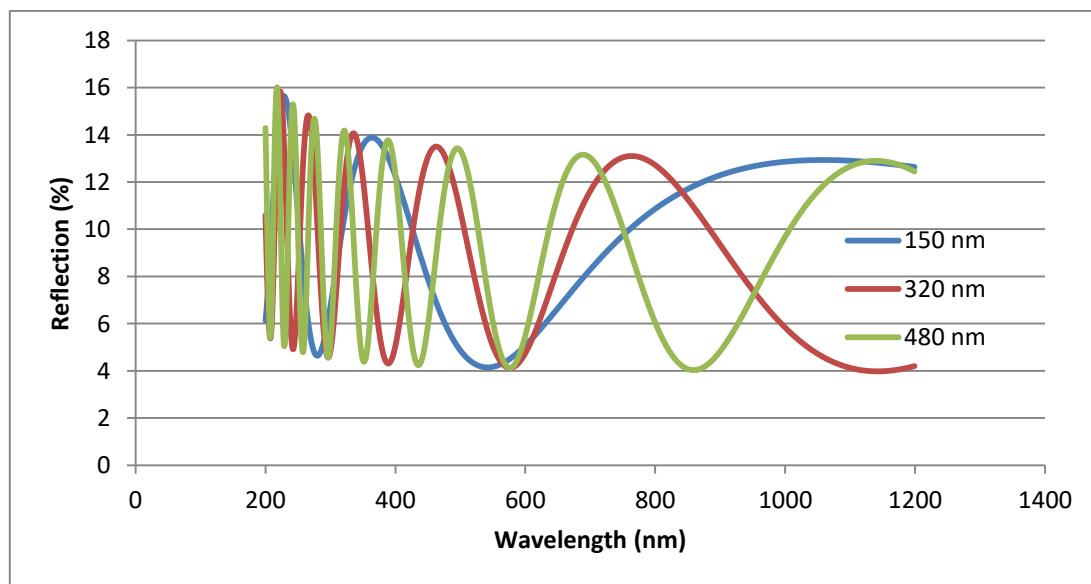


Fig 53. Modelled Reflection Data of Different AZO Film Thicknesses on Corning Glass [269]

It can be observed from the modelled data that with increasing film thickness the level of oscillation observed increases significantly. This leads to the conclusion that whilst thick films are superior from an electronic point of view, they lead to a compromise in the transmission properties due to an increase in overall reflection.

Also of interest is the possibility to extract a value for refractive index from the interference fringes found in the data from the 300 W deposited AZO film. This is possible using the measured reflectance data shown in Fig 54 and equation 4.4 which is based on the Fresnel equations [228].

$$n = \left(\left(\frac{N(\lambda_1 \cdot \lambda_2)}{2(\lambda_1 - \lambda_2)t} \right)^2 + \sin^2 a \right)^{1/2} \quad (4.4)$$

where n is the refractive index, N is the number of observed fringes, λ_1 and λ_2 are the maximum and minimum of the wavelength range respectively, t is the film thickness and a is the angle of incidence of the probe beam.

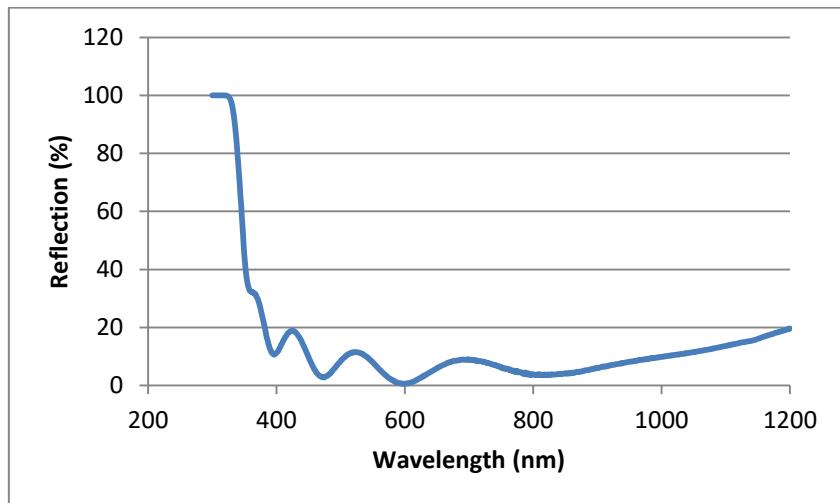


Fig 54. Reflection data for 300 W deposited AZO on Corning 1737 glass

In the case of the data shown in Fig 54, taking the wavelength range to be 400-800 nm, there are 3 observable fringes. Inputting these parameters, the film thickness of 466 nm and the normal angle of incidence into equation 4.4 gives a refractive index of 2.575. This value is slightly higher than that of 2.3 found in [270], however, substrate deposition temperature is known to have an effect on refractive index. Given that the deposited film in Fig 54 was prepared at a deposition temperature 60 °C higher than the film mentioned in literature, it is believed likely that the calculated value is broadly within the range that would be expected.

Whilst not trivial, results suggest it is possible to deposit AZO relatively straightforwardly and with repeatability. Clearly deposition power and pressure have some effect on the resistivity of the AZO films, however the most critical variable is temperature, with an improvement of two orders of magnitude between room temperature deposition and that of approximately 260°C. This temperature range, whilst reasonable high, remains compatible with many low cost substrates and is unlikely to interfere with any other thermal process steps required.

Optical performance varies less significantly than electrical properties with total variation across all the variables being less than 10% (91%-83%) as a percentage of the transmittance of uncoated Corning 1737. Transmission is notably superior in rough films but deposition conditions that yield this film morphology exhibit inferior electronic performance. This suggests that texturing of optimal electrical films might be a viable means to improve light trapping and resultant transmission, which is in agreement with literature [271][272][273].

4.4. Emitter Formation by CVD

The existing emitter formation available at LSBU was by ECR-CVD deposition of silicon layers from SiH₄ with doping achieved by addition of PH₃ to create n-type material. As described in an earlier chapter, ECR-CVD makes use of a highly directional plasma stream which is potentially problematic for achieving conformal growth on non-planar surfaces.

The viability of using this technique to deposit emitters on the pillar structured samples described in chapter 5 was unknown and thus a number of depositions were carried out to assess the resulting silicon layers. Whilst CVD growth on pillars is ultimately demonstrated, it is intended only as a means to assess the performance of the deposition process rather than its capability to produce functioning devices and no working devices were ultimately prepared by this approach.

Prior to deposition, samples were subjected to the standard ultrasonic acetone clean process and piranha etch to remove organic contamination. In addition to the usual processes, samples were placed in a 2% HF solution for 2 minutes prior to loading into the ECR system to remove the native oxide which forms on the surface of silicon. This process improves the quality of deposited silicon by ensuring growth occurs in contact with bare silicon wafer rather than a thin layer of silicon oxide.

PARAMETER	VALUE
Set Heater Temperature	750 °C
Process Pressure	10 mTorr
H ₂ Flow Rate	20 sccm
SiH ₄	1.5 sccm
Microwave Power	800 W
Growth Time	30 minutes

Table 3. Deposition conditions for intrinsic silicon prepared by ECR CVD

After loading to the ECR system, the samples were heated to a set temperature of 750 °C with a surface temperature measured by pyrometer of 685 °C. Accurate temperature measurement within the ECR system is difficult due to the non-normal incidence angle of the pyrometer on the sample surface and the challenges of thermocouple measurements in vacuum conditions. It was known however, that the conditions measured were in the correct range normally conducive to growth of silicon. The parameters used for deposition are tabulated in Table 3. It should be noted that no PH₃ was included in the process gas stream

as the purpose of this deposition was to assess growth uniformity rather than electrical performance; therefore it was not necessary to include the dopant element.

The resulting growth was examined by SEM (see Fig 55) to assess the level and conformity of coverage attained. As predicted the high directional nature of an ECR CVD plasma resulted in good silicon growth ($317\text{ nm} \pm 18$) on horizontal surfaces with normal incidence to the plasma stream, however, the vertical pillar surfaces were for all intents and purposes devoid of silicon deposition. The edges of the faceting resulting from the DRIE process showed very minor signs of growth but at an insignificant fraction of the rate of that seen on the horizontal surfaces. This non-uniform deposition was unsuitable for use as an emitter as it left large exposed p-type regions and did not produce the conformal emitter required for an effective radial junction.

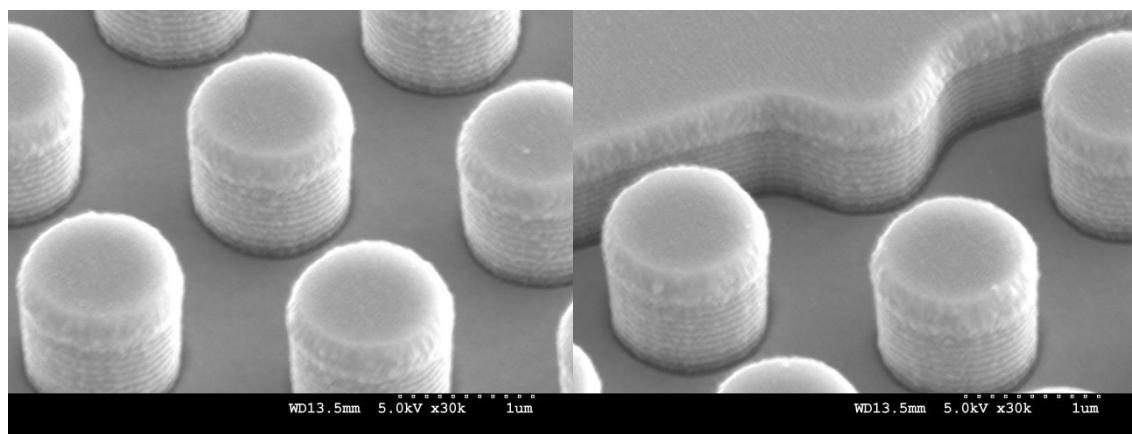


Fig 55. ECR CVD Silicon Growth on Micro-pillar Structured Samples

Whilst not designed for non-plasma assisted CVD deposition, it was decided to briefly investigate whether the ECR system was capable of growing silicon layers by this approach. This process removes the directionality of the deposition process and would potentially be capable of conformal film growth.

Non-plasma assisted CVD film growth typically requires higher surface temperatures than plasma enhanced or ECR CVD as it lacks the pre-cracking of the gaseous species that these processes utilise. The ECR heater was not designed with such high temperatures in mind and therefore limitations were placed on maximum heater temperature and growth times to protect the system. It was initially decided to run at a lower set temperature of $650\text{ }^{\circ}\text{C}$ compared to the previous ECR deposition but to increase the growth time to 60 minutes (see Table 4).

So as not to unnecessarily expend structured samples, only planar samples were used for this deposition to establish if any deposition might occur and if so what thickness of material

was achievable. To this end a masked sample was included to produce a step in any deposited film and allow the thickness to be characterised by stylus profilometry. The complete process conditions for this deposition are listed in Table 4.

PARAMETER	VALUE
Set Heater Temperature	650 °C
Process Pressure	10 mTorr
H ₂ Flow Rate	20 sccm
SiH ₄	1.5 sccm
PH ₃	0.1 sccm
Microwave Power	N/A
Growth Time	60 minutes

Table 4. Deposition conditions for first attempt at preparing n-type silicon by LPCVD

The initial growth parameters resulted in a film with an average thickness of 14.35 ± 3.16 nm. SEM imaging of this film was inconclusive regarding the level of coverage so a second run was undertaken with increased growth temperature, chamber pressure and silane flow rate to attempt to attain an improved deposition. The parameters for this run are given in Table 5. The original intention was to run with a process pressure of 20 mTorr, however, it was noted that at this increased pressure an unacceptable level of load was placed on the turbomolecular pump. The pressure was reduced until the load fell to an acceptable level with a resulting process pressure of 17 mTorr.

PARAMETER	VALUE
Set Heater Temperature	750 °C
Process Pressure	17 mTorr
H ₂ Flow Rate	20 sccm
SiH ₄	3.0 sccm
PH ₃	0.1 sccm
Microwave Power	N/A
Growth Time	60 minutes

Table 5. Deposition conditions for second attempt at preparing n-type silicon by LPCVD.

This run featured increased heater temperature and process pressure in an attempt to increase the resulting film thickness

The second growth regime resulted in a measured film thickness of $77.25\text{ nm} \pm 10.31\text{ nm}$ with associated visible deposition by the naked eye on the surface.

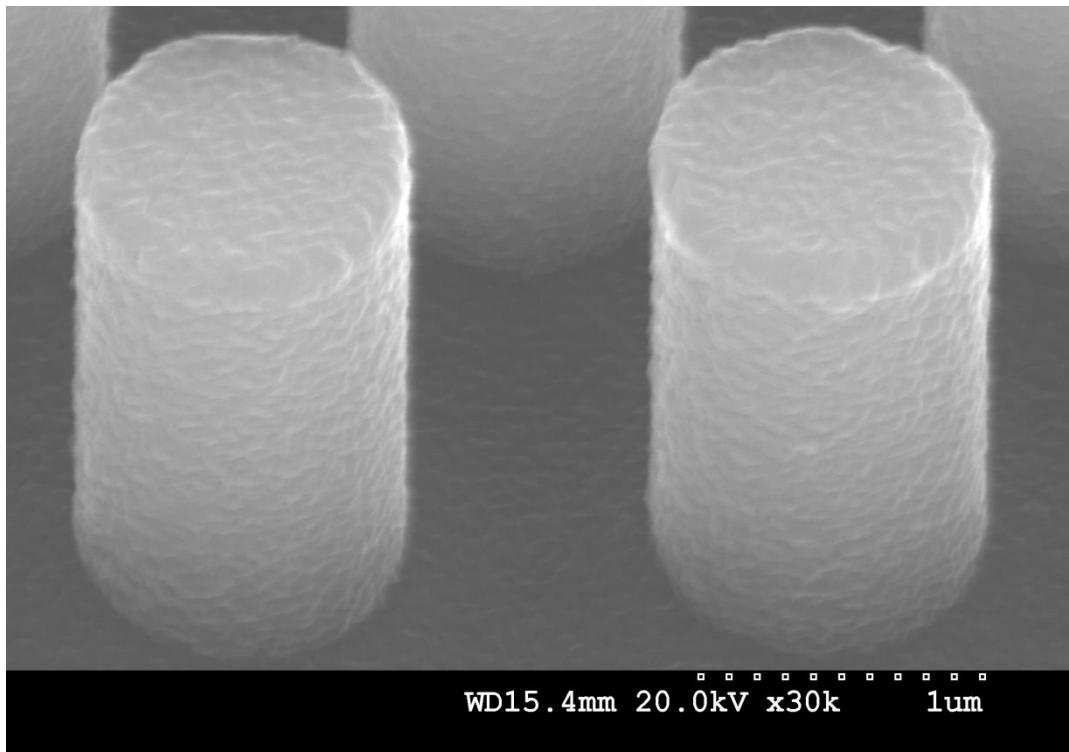


Fig 56. LPCVD Silicon Growth on Micro-pillar Structure Samples

Examination by SEM (see Fig 56) revealed a conformal silicon film with good coverage and visible grain growth.

Electronic analysis of the film was less encouraging, with sheet resistance values in the region of $1000\text{ }\Omega/\square$ suggesting poor phosphorus incorporation from the phosphine source. It is worth noting that the grown layer was found by Raman spectroscopy to be a mix of amorphous and microcrystalline silicon and therefore likely to demonstrate poor electronic performance for these reasons alone, irrespective of doping level.

In an attempt to improve dopant incorporation into the grown emitter, the previous run parameters were repeated but with the phosphine increased to 3 sccm from the previous value of 0.1 sccm. Despite running this process for 60 minutes, visual analysis of the sample surfaces and subsequent examination by stylus profilometry yielded no measurable deposition indicating that the incorporation of this amount of phosphine was sufficient to completely retard deposition.

A further repeat of the run but with 1.5 sccm of phosphine did indeed yield a film, this time of $63.1 \pm 53.8\text{ nm}$. Analysis of the film by four point probe demonstrated very poor electronic

uniformity over the deposited area with values as low as $\approx 20 \Omega/\square$ and as high as $\approx 1500 \Omega/\square$.

Measurement by Suns-V_{oc} (Fig 57) demonstrated that the areas of the emitter with low sheet resistance yielded photo-activity, albeit with marginal performance. Whilst the accuracy of the values is questionable, the suggested value of 1×10^{10} atoms/cm³ for carrier density (compared to 1×10^{13} atoms/cm³ for diffused emitters in this project) suggests that there is inadequate overall dopant incorporation. As it has already been demonstrated that increasing the phosphine content in the growth regime retards deposition, it is unlikely that this deposition process would yield an ideal emitter whilst remaining within the operating limits of the system. The low effective lifetime suggested by the Suns-V_{oc} is as would be expected for a multi-crystalline silicon film as the large number of grain boundaries tends to result in short carrier diffusion length and resultantly lifetime.

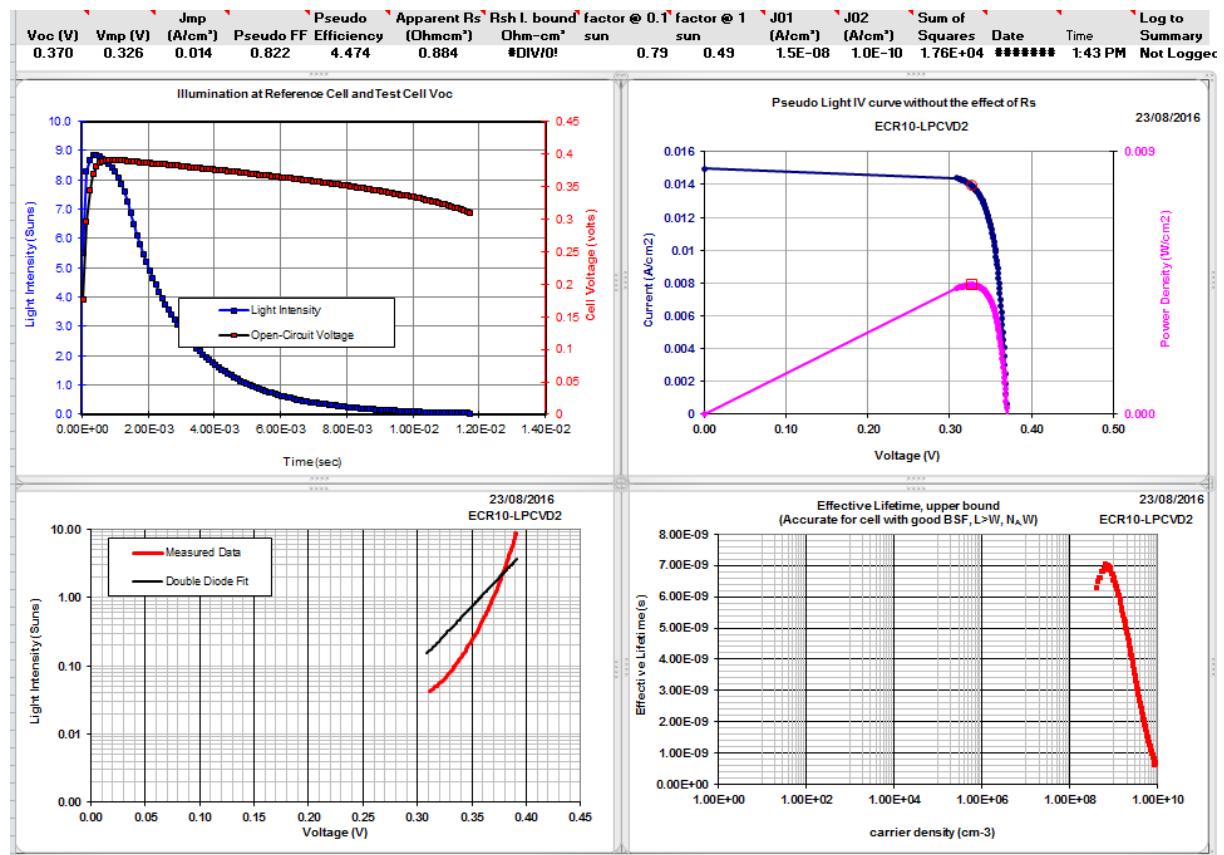


Fig 57. Suns-V_{oc} of the non-plasma assisted CVD deposited n-type silicon emitter with 1.5 sccm of phosphine. The film demonstrated poor uniformity of sheet resistance and the result shown is for an area of low resistance. The Suns-V_{oc} indicates that the area probed is photoactive but the predicted V_{oc} is low and the peak indicated value for carrier density of 1×10^{10} atoms/cm³ is low compared to 1×10^{13} atoms/cm³ for diffused emitters in this project, suggesting that there is poor dopant incorporation

4.5. Device Edge Isolation

Junction shunting is a major source of loss in semiconductor devices. Whilst shunting due to poor emitter design or manufacturing problems is problematic, the more immediate consideration is shunting caused by emitter “wrap-around” resulting from the diffusion process. Emitters formed by any variation of gas phase doping are likely to suffer from this as the dopant does not simply form on the front face of diffused wafers but also the edges and to some extent the rear depending on the diffusion configuration.

This will result in the rear side metallisation contacting both the p-type wafer and the n-type emitter resulting in a heavily shunted device. This is commonly resolved by clearly defining the edges of the emitter and substrate through a process referred to as MESA etching.

4.5.1. MESA Isolation

The alternative to preventing diffusion in unwanted areas of a device is to remove it after processing using an approach referred to as MESA isolation. The term MESA refers to a landform with vertical sides and a flat top from which this process takes its name (seen in Fig 58).

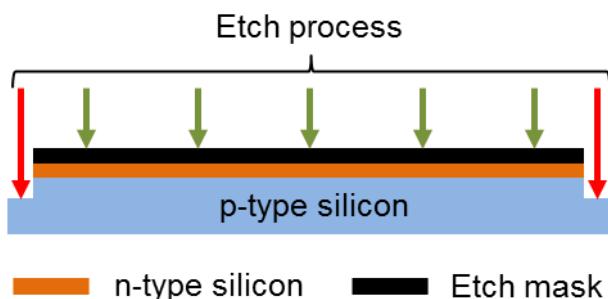


Fig 58. Simplified diagram of the MESA isolation process. The masked area resists etching whilst the edges are removed leaving cleanly defined definition between the two doped regions of silicon.

Commercially this is often achieved by plasma etching; however, it can in principle be achieved by any masking and etching means. Whilst this is relatively trivial for planar devices, achieving a contiguous mask over structured devices required further development. The etch of choice to be employed was a 1:1:2 ratio of hydrofluoric acid, nitric acid and acetic acid commonly referred to as HNA etch. This effectively etches silicon but is also highly aggressive towards a significant number of other materials making mask selection non-trivial.

It was known that photo-resist was incapable of surviving more than brief contact with HNA, ruling out this common mask. It was thought that a hard mask might be a viable solution with chromium known to be resilient to HNA and its application by sputter coating was investigated.

It was found by SEM examination (see Fig 59) that it was effectively impossible to achieve a conformal chromium coating on the structured devices due to the directionality of the deposition process. It would theoretically have been possible to achieve complete masking of the structured devices by depositing a chromium layer that was thicker than the length of the pillars. However, whilst this might have been reasonably practical for the 1 µm length pillars, the 2 µm length pillars would require at least twice the deposition time and the 10 µm diameter pillars with 1:1 and 2:1 aspect would be completely impractical to fully encapsulate.

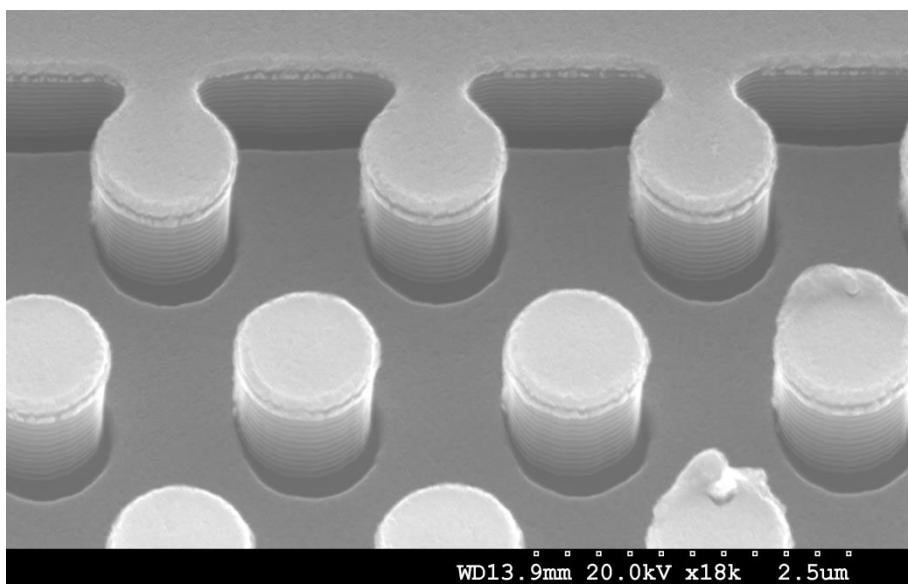


Fig 59. SEM image of a sputtered chromium mask on a pillar device highlighting the problematic nature of achieving conformal coatings by this technique

The other possible solution would be silicon nitride (SiN) which is highly resilient to many etches due to the strength of the nitrogen bonds. However, as had previously been found, SiN by sputter deposition is not effective at resisting etches and would also likely suffer the same lack of conformity as demonstrated by the chromium layers. CVD deposited SiN would have been the preferable choice but due to equipment limitations it was not available for this project.

A solution was found in the form of Apezion Wax W, commonly referred to as black wax. This is a hydrocarbon based wax which was originally specified for use as a temporary sealant material for vacuum systems. It was subsequently found to be highly resistant to a wide

range of chemicals as well as etch solutions, conveniently including HNA. Despite this resilience, it could be straightforwardly removed by a number of aromatic hydrocarbons or organochlorides (such as toluene or trichloroethane). This method was ultimately utilised as the MESA etching means for fabricated devices and is discussed in greater detail in chapter 6.

4.6. Conclusions

- This chapter has reported on the ancillary techniques required to fabricate a functioning solar cell including front and rear contact formation, emitter formation by ECRCVD and device edge isolation processes.
- Aluminium layers were investigated as rear contacts on p-type silicon wafers. The contacts were prepared by sputtering followed by rapid thermal processing at temperatures up to 600 °C. The best achieved contact resistivities were in the region of $7 \times 10^{-4} \Omega \text{ cm}^2$; these fall somewhat short of the best values found in literature of $\approx 1 \times 10^{-4} \Omega \text{ cm}^2$ indicating a need for further refinement.
- Nickel silicide contacts were studied as front surface contacts and shown to provide an effective means of contacting n-type silicon. Their performance demonstrated good resilience to a wide range of processing conditions making them suitable for the devices studied in this work.
- A detailed study on the growth by RF sputtering of aluminium doped ZnO (AZO) films was carried out as a function of growth temperature, deposition pressure and RF power. Electronically optimised AZO was attained, with a resistivity of $4.74 \times 10^{-4} \Omega \text{ cm}$. This is broadly comparable to the best results found in literature. The optical transmission of these films in the visible region was in the range 78-88%. Optical performance was found to vary less significantly than electrical across the range of deposition parameters studied.
- A study of emitter formation using n-doped silicon films grown by ECR CVD and low pressure CVD showed that ECR CVD layers produce non-conformal coverings on the micro-pillar structures under investigation. Films prepared by low pressure CVD are conformal but demonstrate insufficient uniformity and dopant incorporation to be effective as emitter layers without further development.
- MESA isolation by wet etching was found to be an effective means of preventing device shunting but is reliant on a mask which can achieve a conformal coating over the surface to be protected and which is resilient to the etch used. After investigating a number of mask materials, it was found that Apezion Wax W, commonly referred to as black wax, provided a satisfactory solution.

Chapter 5. Design, Formation and Optical Properties of Micro-rods

The device concept investigated in this body of work is that of a micro-rod structured radial junction silicon solar cell. This arrangement is proposed to be a means to enhance light absorption, carrier generation and overall efficiency of thin film silicon solar cells. The radial junction geometry is advantageous as it decouples the optical absorption distance from the carrier collection length; light absorption can take place over the full length of each rod whilst carriers need only diffuse a maximum of half a rod diameter to reach the junction. Rod or pillar structures have also demonstrated anti-reflective properties by increasing light trapping within the inter-pillar area with associated improvement in device absorption.

This chapter will:

- Detail the micro-rod and radial junction device geometry and operation
- Discuss the design considerations involved in the selection of the prepared micro-pillar dimensional parameters
- Describe the process used to prepare the structured samples
- Discuss the visual appearance and optical performance of the as manufactured pillar samples
- Compare optical performance of the manufactured devices with FDTD models with equivalent geometries

5.1. Radial Junction Geometry and Operation

Structured Si solar cells show good potential as a means to enhance thin film cell performance and reduce the quantity and quality of raw material required. Vertically arrayed nano and micro scale pillars based on the radial junction geometry (Fig 60) have two key advantages. First, they have reduced reflection compared to planar Si over a wide range of the optical spectrum [274]. Secondly, they decouple the photon absorption length from that of the carrier collection distance [275]. This relaxes the requirement for long carrier lifetimes and permits lower quality Si to be used which reduces material costs [93].

There has been significant work in the area of nano-scale structures prepared by a variety of techniques and covering much of the dimensional variable space. Structuring schemes of this scale demonstrate excellent anti-reflective and light trapping properties with light absorption values in the region of 99% being achievable [276].

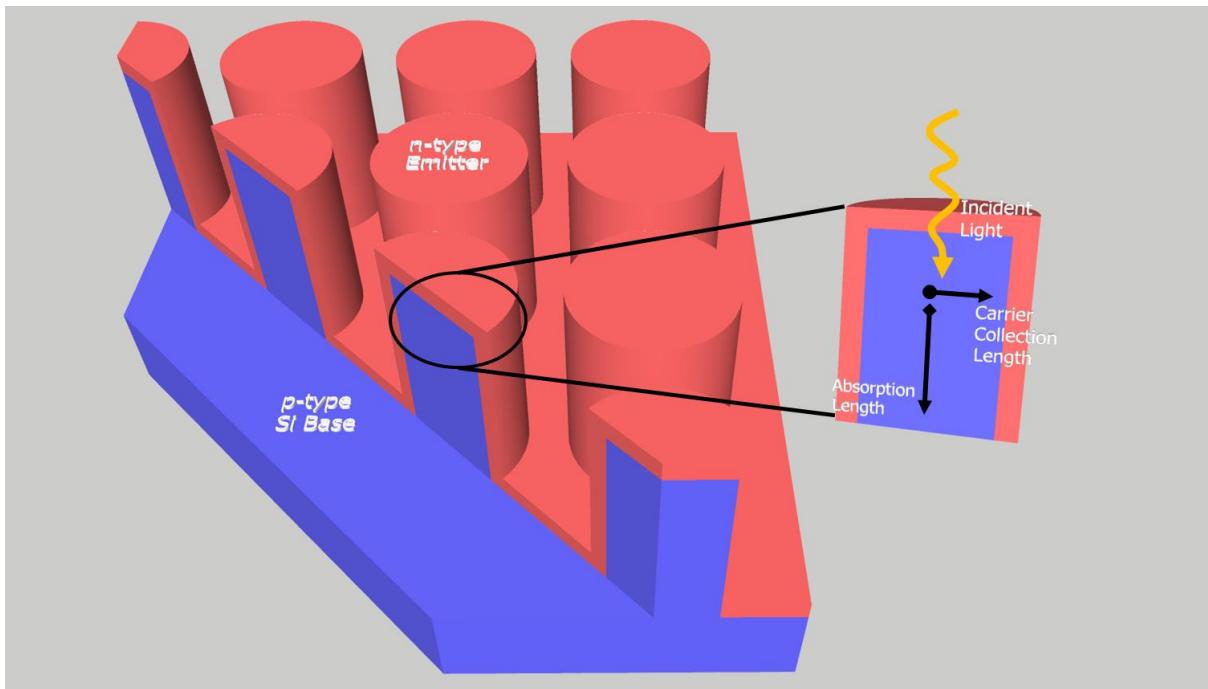


Fig 60. Radial junction solar cell configuration showing the conformal emitter over the structure substrate and highlighting the decoupling of the optical absorption length and that of the carrier collection length

The optical properties of such approaches are receiving significant attention, with the optimisation of dimensions and geometry for structures in the nano-scale being substantially addressed from a modelling approach. Some studies have indicated that disordered arrays may provide superior performance to that of ordered structures [106], whilst others indicated that disordered location of nanostructures has a lesser effect on the absorbed spectrum [277].

Investigation of ordered arrays has demonstrated that structured silicon surfaces have significantly reduced reflection compared to planar silicon films of equivalent thicknesses. The studies indicate that the properties of the arrays are dependent on a variety of factors including the diameter and length of features, their periodicity and their surface filling fraction [278].

The majority of work reported on nano-scale structures previously has focused on their optical properties with less focus on electronic performance. That which has been carried out indicates the large surface area of nano arrays causes high surface recombination velocity with a corresponding reduction in charge carrier collection [279][280]. Effective doping of nano structures is also problematic with tight tolerances on dopant concentration and junction depth required to prevent carrier depletion [281].

Fewer studies have been carried out on micro-scale pillar structures, with those that have been undertaken being predominantly of the experimental approach and from an electronic point of view. Despite this, arrays of organised pillars with V_{oc} values near 600 mV have been demonstrated [128][134] which is a significant improvement over nano-scale structures. Junction formation by both grown and diffused emitter was undertaken and demonstrated the potential advantages to improved electronic performance of micro-scale structures.

This chapter focuses on the development of features on the low micron scale which are readily fabricated by commercially viable processes. These larger features require fewer complex and failure prone process steps for device fabrication resulting in more straightforward production.

5.2. Design of Micro-pillar Test Cell Substrates

When considering the geometry and dimensions of the pillar arrays it was necessary to balance optical enhancement and electronic performance. Whilst larger pillars could result in better electronic performance, if they were excessively sized then there would be little or no optical benefit and the advantages of the radial junction geometry would be negated.

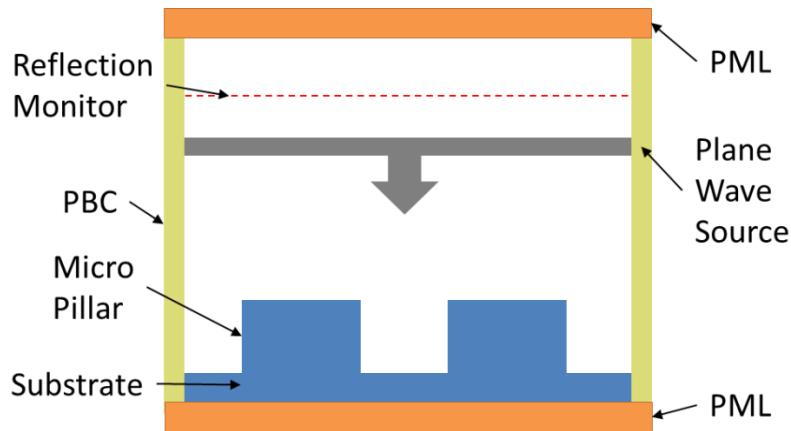


Fig 61. Representation of the FDTD configuration used to model the optical properties of the micro-pillar arrays investigated [282]

It was considered that a 1 μm diameter pillar would produce favourable optical absorption, backed up by a preliminary optical modelling study in collaboration with London City University. The modelling was performed at City University using the Lumerical photonic and opto-electronic modelling package, which uses finite-difference time-domain (FDTD) method [283] to solve Maxwell's equations [284] in three dimensions. This allows it to analyse the interactions of ultraviolet (UV), visible and infra-red (IR) radiation with modelled structures.

This capability is used in conjunction with variable position measurement layers to calculate absorption, reflection and transmission and perfectly matched layers (PML) [285] which define boundary conditions for the model and prevent stray electromagnetic radiation from contaminating the solution (Fig 61).

To allow direct comparison, the model was designed to closely match the proposed geometry and dimensions of the pillar samples. By using periodic boundary conditions (PBC) [286] on the edge of the simulation window, it was only necessary to model one complete repeat of any given array configuration to achieve a theoretically infinite array of pillars. Even for a relatively simple model such as this, the computational time to achieve a few picoseconds of simulation time was on the order of 18-24 hours.

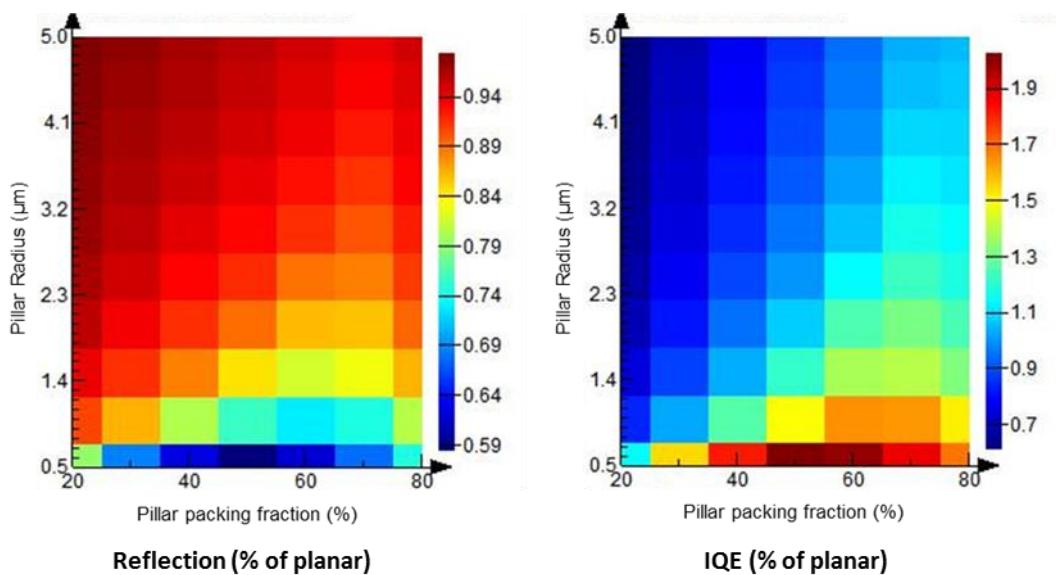


Fig 62. Modelled Reflection and IQE Enhancement of 1 μm micro-pillars (note scale given as 1 = 100%) highlighting the optimal performance of pillars with a small radius and 50-60% packing fraction

The model was re-run multiple times with variations in pillar radius and packing fraction (spacing) to permit an analysis of the proposed designs and inform a decision.

Fig 62 shows the results for reflection and internal quantum efficiency (IQE) of a 1 μm tall pillar cell with varying pillar radii and packing fraction as a percentage equivalent of a planar device. IQE defines the efficiency with which incident photons that are not reflected or transmitted are able to generate collectable charge carriers.

It is apparent that a pillar with 0.5 μm radii or 1 μm diameter gives the best enhancement for reflection (less than 60% of a planar cell). It also indicates that a packing fraction of

approximately 50% gives the best overall enhancement which for a $1\mu\text{m}$ pillar translates to a nominal spacing of $0.25\mu\text{m}$.

It can be noted that as the anti-reflection enhancement falls with increasing pillar radius the severity of the reduction is moderated by increasing the pillar packing fraction. This indicates that the increase in reflection from the greater surface area atop the pillars is partially offset by the improved inter-pillar light trapping.

It follows that reduced reflection and therefore enhanced absorption should improve the IQE of the modelled structures which is in agreement with the presented data. From the IQE graph, a $0.5\mu\text{m}$ radii pillar with 50% packing fraction exhibits a theoretical enhancement of nearly 1.9 (190%) over a planar cell. Whilst unlikely to be achievable in a practical device, this highlights the potential for performance enhancement by utilising microstructures.

A further consideration was whether the pillar array should be arranged in a square or hexagonal fashion. Further simulation by City University indicated that for identical spacing the difference in light trapping was negligible. This was backed up by Li, Yu and Li in their modelling of absorption of periodically structured arrays [101].

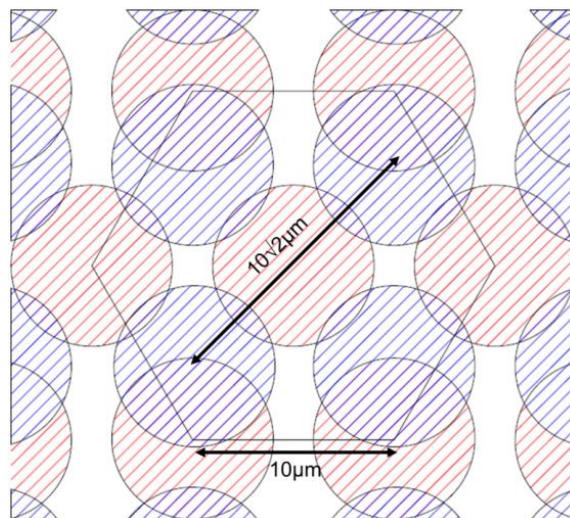


Fig 63. Difference in fill fraction between square and hexagonally arrayed pillars

Ultimately the hexagonal array was chosen on the basis that 47% of the surface was occupied by pillars as opposed to 40% for a square array of with the same pillar edge to edge dimension. This would increase the proportion of light absorption taking place along the length of a pillar rather than the planar areas in between. The example in Fig 63 highlights this, with it being apparent that the hexagonally arrayed pillars all have centre to centre spacings of $10\mu\text{m}$ whilst the square array has adjacent spacing of $10\mu\text{m}$ but diagonal spacing of $10\sqrt{2}\mu\text{m}$ and therefore a lower fill fraction of the surface.

5.3. Substrate Selection

With known values for pillar dimensions, it was necessary to consider the position and width of the depletion region resulting from the formation of junctions on the pillars. This was especially relevant when considering the 1 µm diameter pillars as a poorly conceived junction design could easily lead to a depletion region that exceeds the dimensions of the pillar.

An excel based numerical model was constructed to calculate the diameter and position of a semiconductor junction's depletion region based on the doping concentration of the wafer and emitter. This was based on the equation for depletion region width in an abrupt junction semiconductor:

$$W = \sqrt{\frac{2\epsilon_s}{q}} \left(\frac{N_A + N_D}{N_A N_D} \right) V_{bi} \quad (5.1)$$

[287]

Where ϵ_s is the semiconductor permittivity, q is the charge on an electron, N_A and N_D are the number of acceptors and donors respectively, V_{bi} is the built in voltage potential and W is the total depletion region width.

Once the width of the depletion region is known it is also possible to establish the positional extent of the edges of the depletion region in the n and p regions of the semiconductor by:

$$x_p = W \frac{N_D}{N_A + N_D} \quad \text{and} \quad x_n = W \frac{N_A}{N_A + N_D} \quad (5.2)$$

[287]

where x_p and x_n describe the distance of the edge of the depletion region in the p and n type regions respectively.

Fig 64 plots the width and position of the depletion region in a hypothetical bisected 1 µm pillar with a conformal emitter. The emitter doping was fixed at 1×10^{18} atoms/cm³ as this yielded favourable results in PC1D models and increasing the doping level further in the thin emitter layer had minimal effect on the position and width of the depletion region. It should be noted that the n-type region has been drawn significantly out of proportion for illustrative purposes (note maximum value of 0.004 µm or 4 nm).

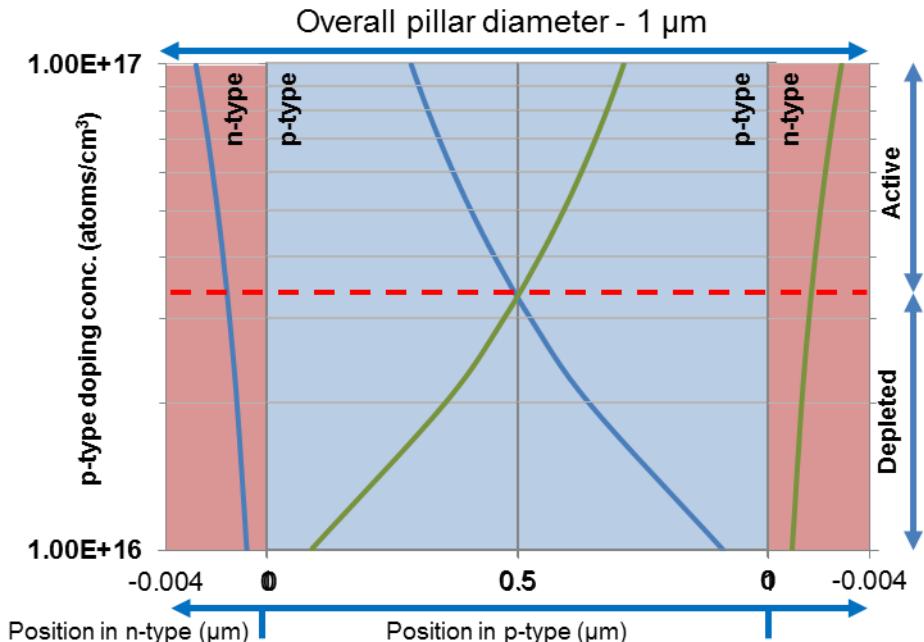


Fig 64. The effect of pillar doping concentration on position of depletion region in a 1 μm micro-pillar. The pairs of blue and green lines indicate the position and width of the depletion region on each side of the structure as a function of base wafer doping concentration and highlight the potential for fully depleted pillars if doping is not considered carefully.

The outer lines (blue on the left and green on the right) show the extent of the depletion region in the n-type emitter whilst the inner lines show the extent of the depletion region in the p-type core. When each pair of coloured lines is considered together they illustrate the width of the depletion region. Any value for base wafer doping where the depletion regions for each side of the pillar overlap (i.e. the blue and green lines cross) will result in a pillar depleted of minority charge carriers. As recombination is generally more severe in the depletion region [288], generated carriers have a higher chance of recombining without being collected. A device which consists of overlapped depletion regions is therefore considered electronically compromised and undesirable, particularly from a PV point of view.

The minimum preferred doping value was calculated to be in the region of 4×10^{16} atoms/ cm^3 (shown by the hashed red line in Fig 64) which equates to a resistivity of $0.4 \Omega/\text{cm}^{-1}$. As a result, wafers with a resistivity range of $0.1\text{-}0.5 \Omega/\text{cm}^{-1}$ were specified as they would be adequate for the $1 \mu\text{m}$ pillars with careful control of the emitter doping and entirely suitable for the $10 \mu\text{m}$ pillars. Selecting a more highly doped base wafer would reduce the chances of overlapping depletion regions but could itself result in performance losses as there would be higher bulk recombination due to the increased doping level.

5.4. Pillar Formation

Due to equipment limitations at LSBU, the masking and etching of the structured samples was carried out in collaboration with Philips Innovation Services at MiPlaza as part of the EUMINAFab Europe wide open access scheme. This collaborative partnership of academic and industrial facilities provides access to a wide array of high tech facilities and experts to carry out fabrication or characterisation which would otherwise be beyond the scope of most research groups. In the case of this project it permitted the masking, patterning and DRIE etching of relatively large (18 mm x 18 mm) samples with finish quality and repeatability not achievable at LSBU.

The fact that the work was done externally also dictated the maximum achievable etch depth and therefore pillar length to that achievable by the equipment at MiPlaza. This turned out to be a 2:1 aspect ratio, i.e. 2 µm length for the 1 µm diameter pillars and 20 µm length for the 10 µm diameter pillars.

Table 6 lays out the various array configurations, pillar diameters and etch depth combinations that were specified for production by MiPlaza. It may be noted that position 1 for the 1 µm pillars has no value. This is due to limitations in the masking process which meant that 0.25 µm spacing was effectively unachievable.

Fig 65 illustrates the layout of structured samples on a 150mm, <100>, p-type silicon wafer. The larger samples measure 18 mm x 18 mm and are intended for characterisation purposes whilst the smaller samples are 9 mm x 9 mm for production of electronic test cells. The red dashed lines indicate where the wafer will be laser scribed to allow easy separation of samples. A 2 mm planar gap, indicated by green hashing, is left around the etched areas to allow for contacting and handling of the samples.

Wafer ID.	Pillar Dimensions		Pillar Spacing			
	Pillar Diameter	Etch Depth	Position 1	Position 2	Position 3	Position 4
111A	1 µm	1 µm	N/A	0.5 µm	0.75 µm	1 µm
111B	1 µm	1 µm	N/A	0.5 µm	0.75 µm	1 µm
121A	1 µm	1.5 µm	N/A	0.5 µm	0.75 µm	1 µm
131A	1 µm	2 µm	N/A	0.5 µm	0.75 µm	1 µm
131B	1 µm	2 µm	N/A	0.5 µm	0.75 µm	1 µm
212A	10 µm	10 µm	2.5 µm	5 µm	7.5 µm	10 µm
212B	10 µm	10 µm	2.5 µm	5 µm	7.5 µm	10 µm
222A	10 µm	15 µm	2.5 µm	5 µm	7.5 µm	10 µm
232A	10 µm	20 µm	2.5 µm	5 µm	7.5 µm	10 µm
232B	10 µm	20 µm	2.5 µm	5 µm	7.5 µm	10 µm

Table 6. Pillar array geometry and spacing details

The pillars were prepared by optical lithography and deep reactive ion etching (DRIE) on 150 mm p-type silicon wafer. To facilitate the low micron scale patterning over a relatively large area, stepper lithography [289] is utilised for patterning the wafers prior to etching. The stepper system uses a negative mask referred to as a reticle which is a 5:1 enlargement of the mask size required for the actual patterning. The pattern is then focused onto the layer of resist atop the wafer through a series of reduction and focusing lenses to produce a 1:1 replication. Rather than use the resist directly in the DRIE process [290], it is used to pattern an oxide based hard mask [291] which has superior etch selectivity. Upon completion of the etch process, the hard mask is removed leaving the prepared pillars (Fig 66). By this method it would in principle be possible to apply the structuring over the full area of a 150 mm wafer.

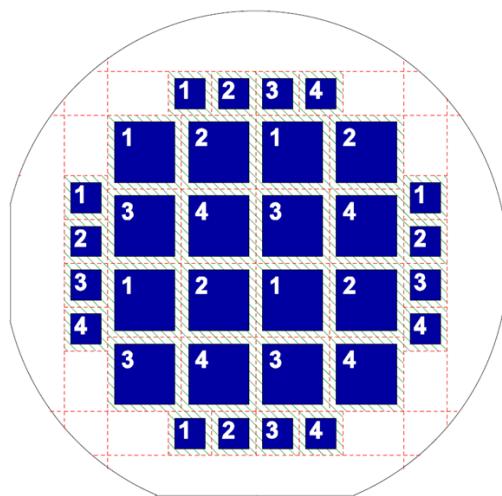


Fig 65. Schematic layout of structured areas on 150 mm diameter wafer

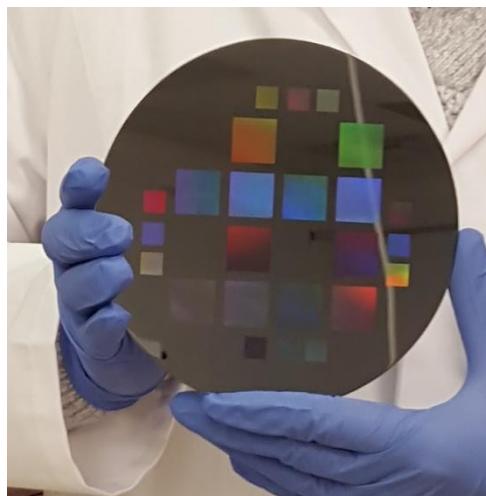


Fig 66. Photograph of a complete structured wafer

5.5. Post Formation Inspection by SEM

After manufacturing the micro-pillar structured samples properties were assessed by scanning electron microscopy (SEM) at LSBU. The structures were found to be uniform and periodic with few observable defects.

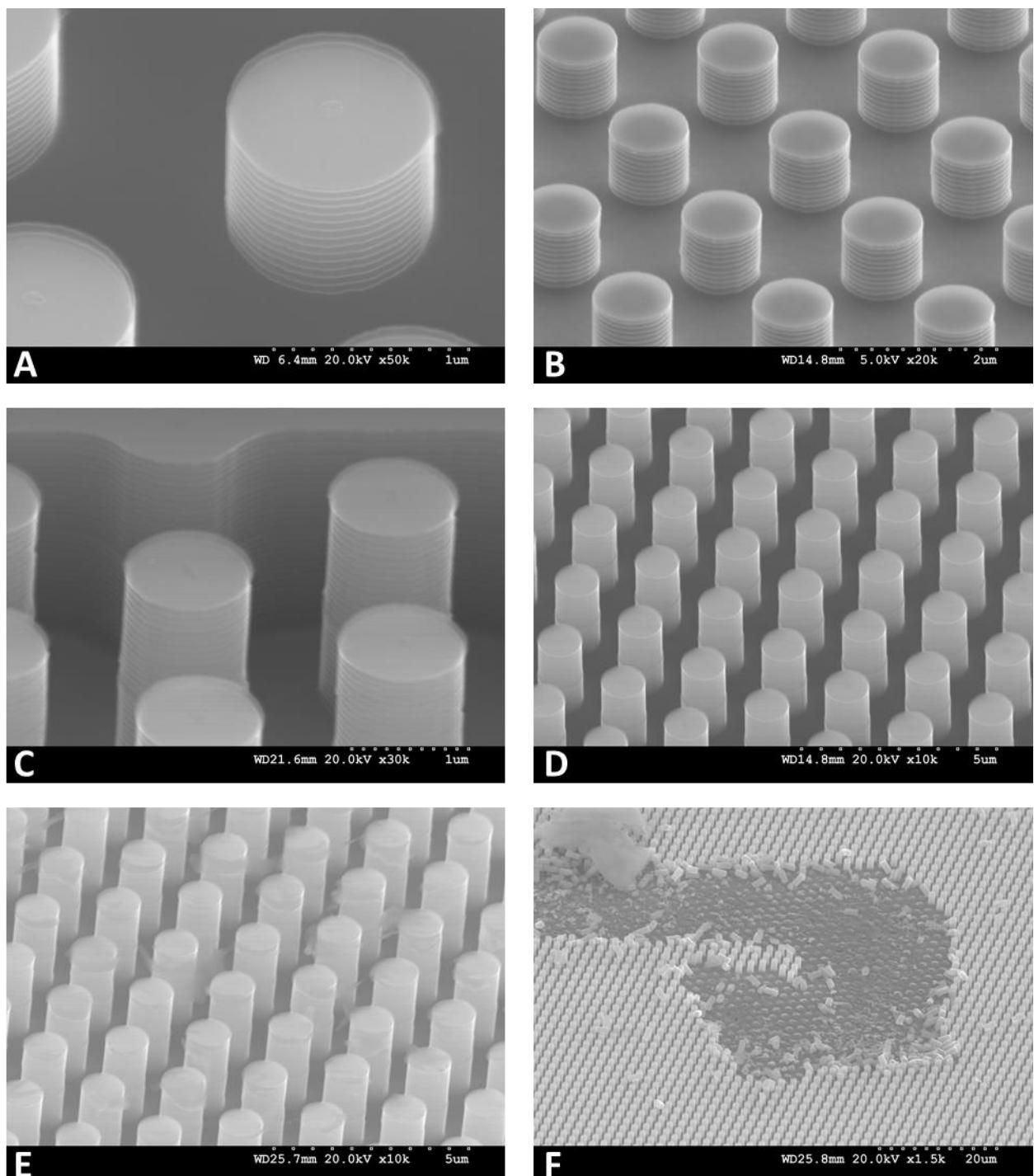


Fig 67. Initial Pillar SEM Examination. **A&B.** 1 μm diameter, 1 μm height pillars **C&D.** 1 μm diameter, 2 μm height pillars **E.** Material left from the etching process **F.** Pillar damage

Examination of the pillar structures highlighted various structural phenomena of interest. Perhaps the most obvious feature is the periodic faceting of the vertical sides of the structures (Fig A & B of Fig 67). This results from the repeated etching and passivation cycles inherent to the DRIE etching process. It was further noted that on the 1 μm and 10 μm pillar structures with 2:1 aspect ratio (the taller of each diameter series) there is a slight change in pillar diameter at the mid-point (visible in images C & D of Fig 67). It is believed that this results from a DRIE etch recipe change during the process to maintain its anisotropic nature and prevent side wall tapering. Examination of a random selection of samples highlighted the repeatability and yield of the fabrication process demonstrated by the excellent uniformity of samples and very few defects observed.

Some structures (image E of Fig 67) were observed to have residual material on the surfaces which appeared to have previously been conformal to the surface. This is presumed to have either been left from the masking of the samples or residue from the post manufacturing cleaning steps. Irrespective of the cause it highlighted the need to subject the samples to a stringent cleaning process prior to further processing to prevent contamination or fabrication issues. Whilst the samples were found to be impressively resilient to cleaning and masking processes they were ultimately susceptible to mechanical damage, particularly when mishandled. Extra care was required when using metal tweezers (image F of Fig 68) as even minor contact was capable of causing significant surface damage. This would be particular relevant after emitter diffusion had taken place as the damaged pillars would leave exposed p-type cores with the possibility for severe shunting and performance losses.

5.6. Optical Properties of Micro-pillars

Spectrophotometry was used to examine the optical properties of the 1 μm (Fig 68) and 10 μm (Fig 69) diameter micro-structured samples and assess their level of reflection. A planar silicon reflection profile is included in each graph for comparison.

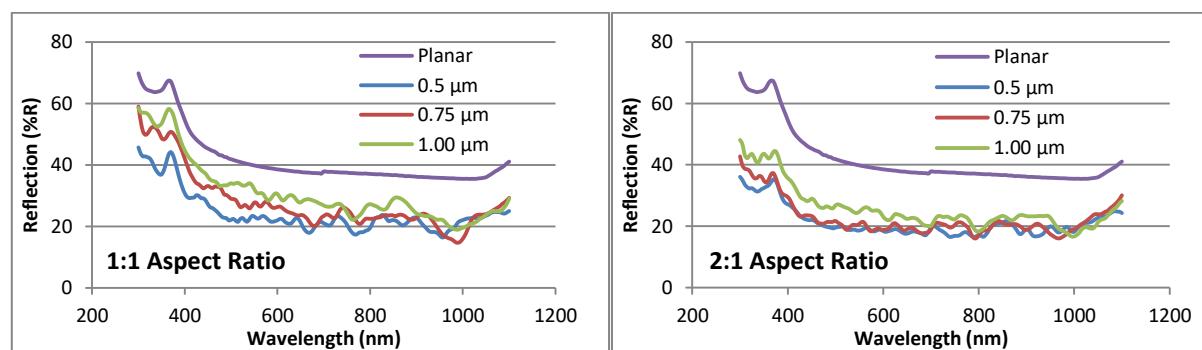


Fig 68. 1 μm Diameter 1:1 & 2:1 Aspect Ratio Pillars %R (Legend describes inter-pillar spacing)

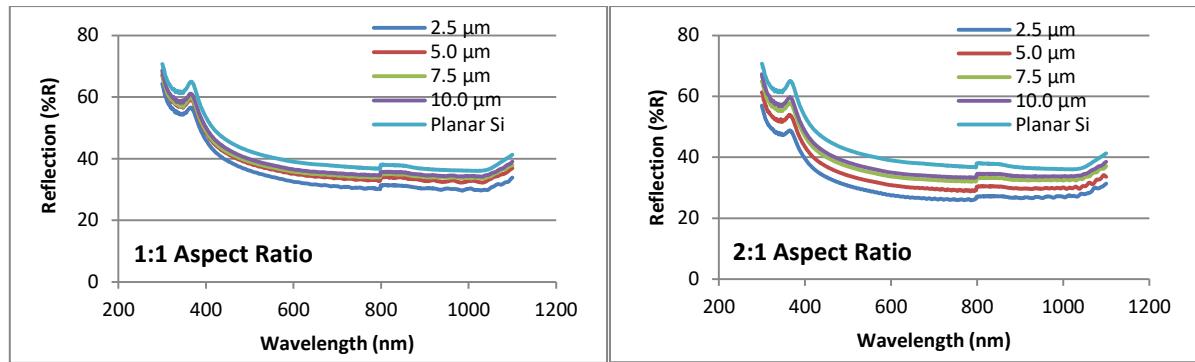


Fig 69. 10 μm Diameter 1:1 & 2:1 Aspect Ratio Pillars %R (Legend describes inter-pillar spacing)

The 1 μm diameter pillar series exhibit high levels of oscillation in their reflection response plots. The coloured patterns visible by the naked eye (Fig 70(a)) would suggest that this is as a result of diffraction and scattering effects caused by the inter-pillar spacings being of a similar order of magnitude of the wavelengths of light being measured.

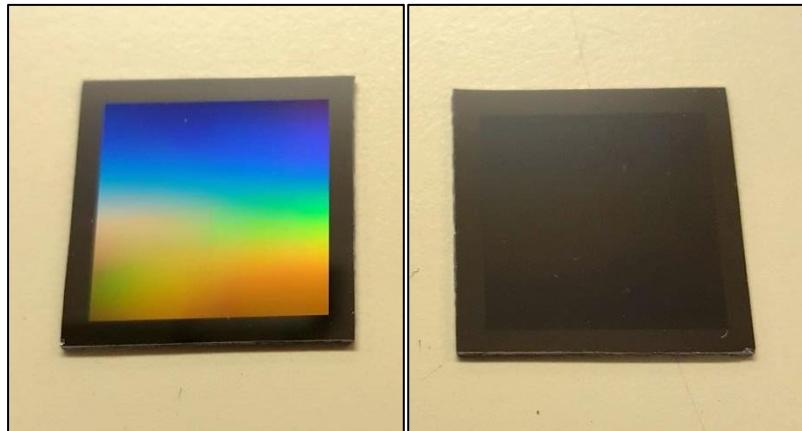


Fig 70. Appearance of (a) 1 μm and (b) 10 μm structured silicon surfaces under ambient light conditions. Note that the blackness of the 10 μm sample is exaggerated by the camera angle and is closer to grey.

The 10 μm pillars exhibit near identical optical profiles to planar silicon but with decreasing reflection proportional to the decreasing pillar spacing. There is minor oscillation observable above 850 nm in the traces (particularly the 2.5 μm and 5 μm samples) where the wavelength becomes a meaningful proportion of the inter-pillar spacing. The observable change in reflection between the 7.5 μm and 10 μm spacing pillars is negligible. This suggests that for pillars with a diameter on this scale or larger, changing the pillar spacing further will not result in significant changes in the anti-reflective properties beyond those that

result from surface roughness that is produced by the fabrication process itself. Looking at Fig 70(b), the diffraction and scattering patterns that are observable by the naked eye for the 1 μm pillars are not present on the 10 μm samples as the inter-pillar spacing's are substantially larger than light in the visible wavelength.

Whilst comparative analysis of the anti-reflective properties of the pillar devices is possible by direct comparison of the spectral profiles, it is perhaps more convenient to be able to consider the reflection of each configuration as a single value. To this end, the area under each sample's reflection spectra was calculated using integration under the curve. This was then normalised to the area under a planar sample spectra to produce a value for reflection as a percentage of a planar sample. Furthermore by plotting these values against fill fraction, that is the ratio of space filled by pillars to space between pillars, instead of edge to edge spacing it is possible to directly compare the reflectivity of the 1 μm and 10 μm diameter pillars on the same plot (Fig 71).

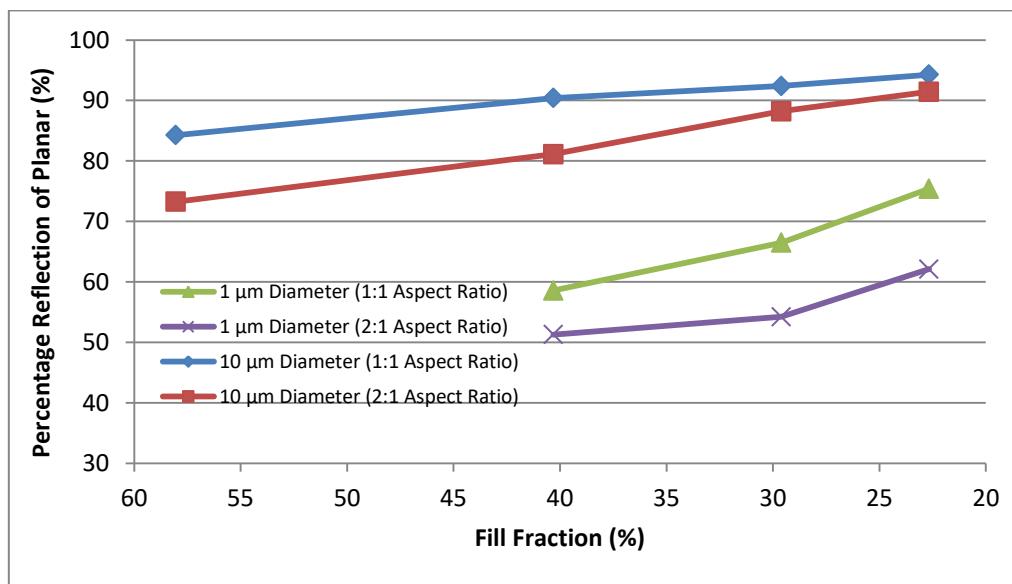


Fig 71. Percentage reflection of pillar samples relative to that of a planar sample and plotted against fill fraction of pillars

As predicted by the initial FDTD modelling the optimal region for anti-reflection enhancement is in the 40-60% fill fraction region with all samples in the region showing the lowest reflection compared to the planar control. Poorer performance is noted for the low fill fractions where significant areas of planar silicon at the base of the pillar are exposed to the incident light resulting in increased reflection. This is particularly noticeable for the 10 μm pillars where the substantially above wavelength inter-pillar spacing results in minimal light scattering and trapping to compensate for the large planar surface area between pillars. Notably, at the lowest fill fraction for the 10 μm pillars with both 1:1 and 2:1 aspect ratio the

percentage reflections begin to approach a similar value. This suggests that for large pillars with low packing fractions, increasing the length of the pillars has minimal additional effect on the anti-reflection properties of the structured arrays.

5.7. Comparison of Modelled and Measured Data

After the initial FDTD modelling was used to inform the design parameters of the fabricated pillar devices, the model was expanded to produce complete reflection spectra for all the 1 μm samples. Fig 72 shows the comparison between the modelled and measured reflection data for the 1 μm samples with 1:1 and 2:1 aspect ratio as a percentage of planar device reflection.

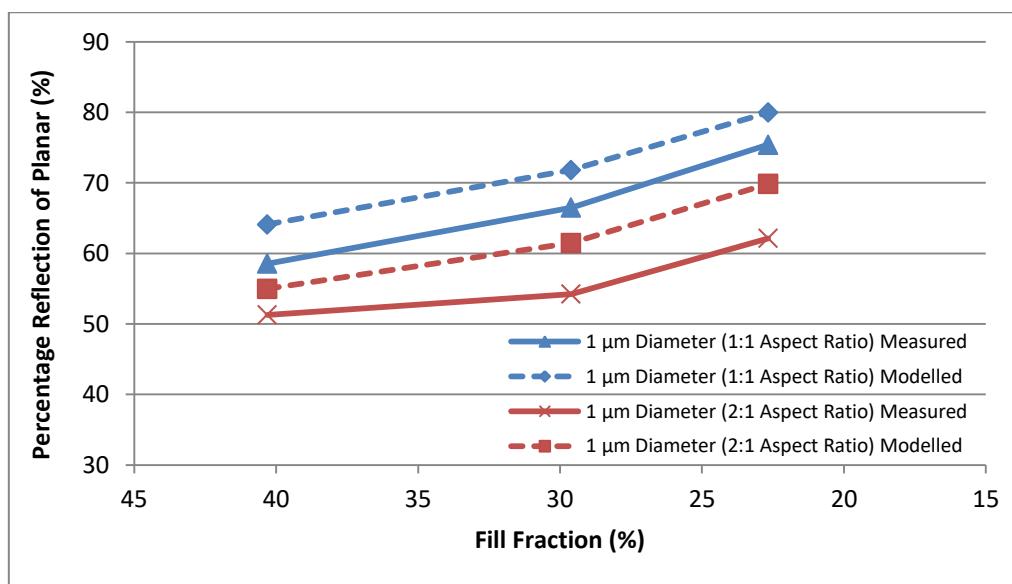


Fig 72. Modelled and measured percentage reflection of 1 μm pillar samples normalised to that of a planar sample and plotted against fill fraction of pillars

It is apparent that the modelled reflection is higher than that of the measured samples for both aspect ratios. It can be suggested from the correlation between the modelled and measured planar sample in Fig 73 that the initial simulation conditions used are appropriate and therefore not at fault for the disagreement. The culprit is in fact believed to be caused by the oscillation noted in the modelled data (Fig 73), which is more substantial than that observed for the measured data. A hypothesis for this phenomenon is that the modelled space between the pillars acts as a cavity with a complex shape and may result in a resonance being created which causes increased oscillation in the reflection properties. Even with the inclusion in the model of the faceting resulting from the DRIE process the modelled surfaces will always be smoother than the real sample surfaces and as such it is likely that modelled samples will always exhibit this increased oscillation over their real world

counterparts. The result of this increased oscillation is a greater area under the reflection spectra for the modelled samples and the associated disagreement between the modelled and measured data when integration under the curve is used for comparison.

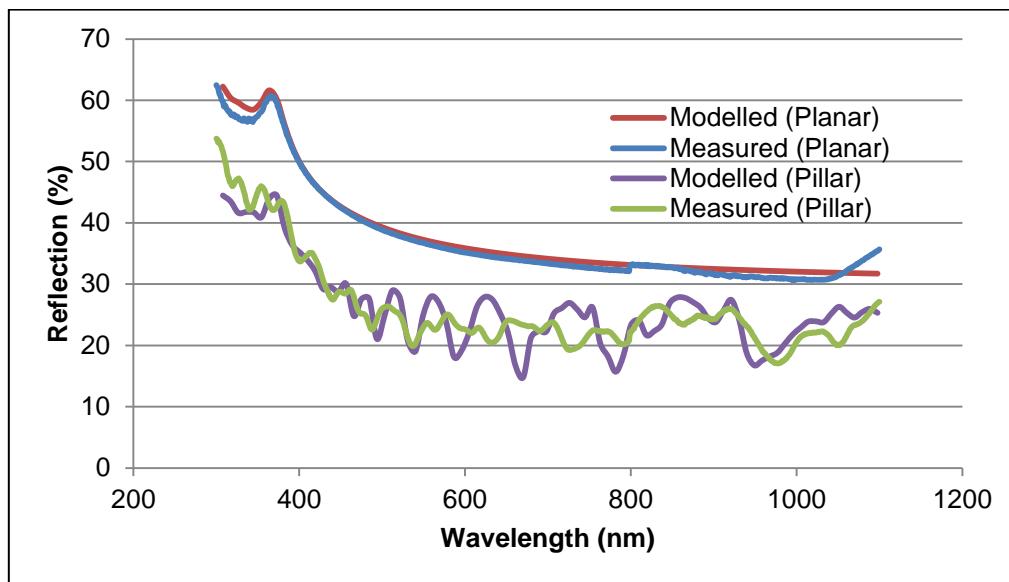


Fig 73. Comparison of the modelled and measured data for a planar silicon sample and a 1 μm pillar with 2:1 aspect ratio and 30% packing fraction

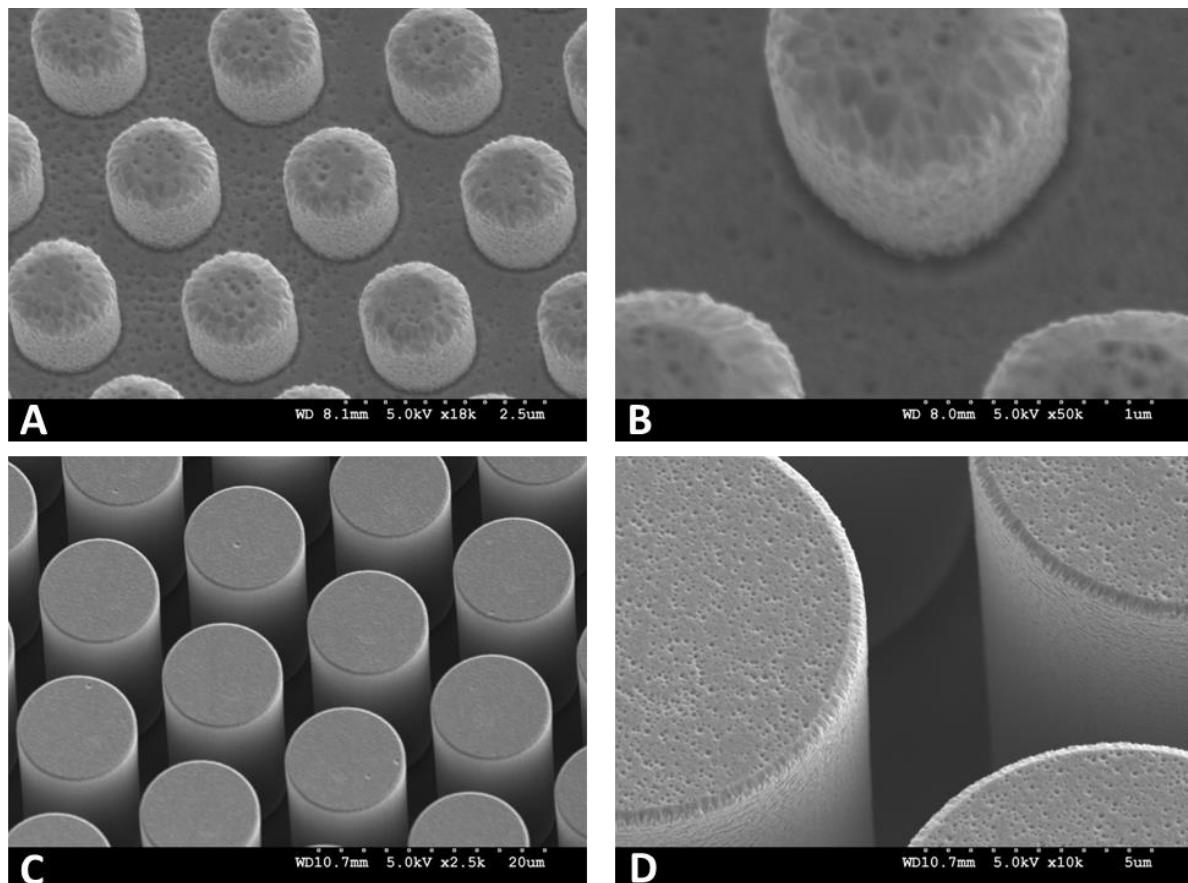
Notably, the measured data sits reasonably centrally on the oscillation exhibited by the modelled devices and demonstrates good correlation when the oscillation is taken into consideration. This level of agreement is noted across all the samples when assessed individually which explains why the disagreement in Fig 72 is present but consistent. As the oscillation is believed to be predominantly a feature of the modelled surfaces, it is likely that the only means of improving the correlation would be to model nanoscale surface roughness. Taking into account the already memory intensive process of modelling the pillars, this is likely to be unachievable with the available hardware and therefore an alternative approach would need to be considered.

It would have been useful to compare modelled and measured data for the 10 μm diameter pillars; however, due to the significant increase in model size as a result of the larger features it was not possible to do so with the available computer hardware.

5.8. Optical Properties of Samples Coated with AZO

Whilst the primary function of applying aluminium zinc oxide (AZO) to the surface of the structured samples post device fabrication is to act as a transparent conductive oxide (TCO), it has also been noted that AZO possesses useful anti-reflective (AR) properties.

It was initially unknown how effectively AZO could be deposited onto the structured samples as based on the chromium masking work seen in chapter 4, there was the possibility that the directionality of the process would result in non-uniform coverage. The key difference with the deposition of optimised AZO, however, is the effect that the raised substrate temperature (≈ 260 °C) has on the surface energetics. The increased surface energy appeared to permit the effective self-organisation of the sputtered layer during deposition and resulted in high quality, uniform films as can be seen in Fig 74.



**Fig 74. SEM Images of AZO Coated Pillars. A&B – 1 μm diameter, 1:1 aspect ratio
C&D - 10 μm diameter, 2:1 aspect ratio**

Fig 75 highlights the reflection spectra of an uncoated polished silicon sample compared to identical samples that have been sputter coated with AZO or silicon nitride (SiN), a common material used for AR coatings. It should be noted that silicon nitride prepared by sputter deposition can be inferior to that deposited by chemical vapour deposition and the example shown here is known not to possess the optimum stoichiometry. However, it demonstrates that, for films deposited by sputtering, it is possible to achieve better AZO anti-reflective coatings than SiN.

Furthermore, the electronically optimised AZO shown (thickness of 466 nm and resistivity of $4.74 \times 10^{-4} \Omega \text{ cm}$) is known not to be the ideal thickness for best AR properties. Despite this it still demonstrates a good enhancement over both the un-optimised SiN and the polished silicon. To assess the best possible AZO performance from a purely optical point of view, the optimised thickness was calculated and applied by sputtering to a polished silicon sample.

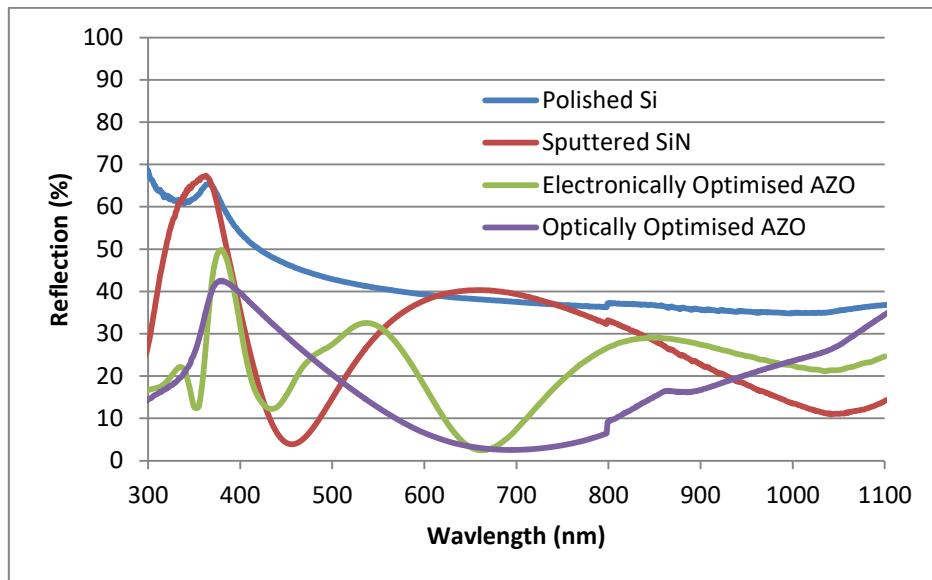


Fig 75. Reflection spectra of SiN and AZO coated silicon and uncoated polished silicon

It can be observed from Fig 75 that there is quite significant additional AR capability that can be achieved by optimising the AZO layer. However, at the optimal thickness of ≈ 80 nm the resistivity of the film rises to $7.27 \times 10^{-3} \Omega \text{ cm}$, over an order of magnitude more resistive than the electronically optimised film.

As AZO was to be applied to the pillars as a TCO regardless, it was worth investigating its AR capability at the electronically optimised thickness in conjunction with structures which are themselves designed to possess AR properties.

Fig 76 compares the normalised reflection of uncoated and AZO coated pillar devices compared to polished planar silicon. The addition of the TCO layer to the pillars resulted in a significant reduction in the reflection of the structures. Notably the 1 μm diameter pillars demonstrated sub 30% reflection of planar devices and all structures showed at least a 30% improvement over their un-coated counterparts.

It is of course relevant that this comparison is to polished silicon whilst the AR properties of AZO are significant even on planar silicon as demonstrated by Fig 75. A comparison of the AZO coated pillars with AZO coated planar silicon is shown in Fig 77. In this case the results are interesting as the improvement over planar is much less significant and in the case of the

10 µm diameter pillars, several of the configurations actually demonstrate greater reflection than the AZO coated planar device.

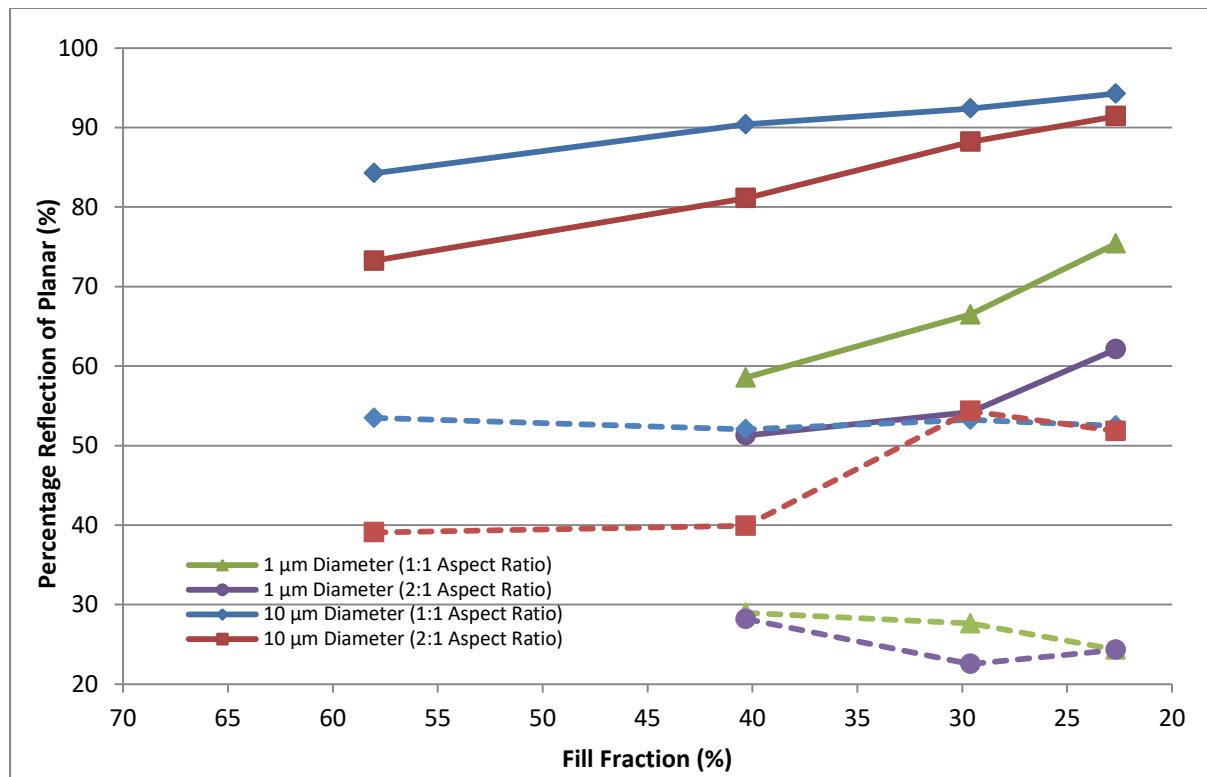


Fig 76. Percentage reflection of all pillar samples normalised to that of a planar sample and plotted against fill fraction of pillars, solid lines represent samples as fabricated whilst hashed lines are samples with AZO coating

Due to the non-optimised nature of the AZO coating there are substantial peaks in its reflection spectrum. At certain points these maxima align with the maximal values of the pillar reflection spectra resulting in levels of reflection as high as that of a planar device or in the case of the 10 µm pillars with 1:1 aspect ratio and two of the four with 2:1 aspect ratio slightly higher than planar. This effect is further demonstrated by the 1 µm pillars with the 1:1 aspect ratio pillars showing decreasing reflection with decreasing fill fraction, the reverse of the expected result. With further modelling of optical parameters and development of the AZO deposition process it is likely that further improvements of the combined AR properties of the pillars and the TCO could be achieved.

It is also worth noting that it does not automatically follow that devices that exhibit poorer optical properties compared to a planar device will exhibit poorer performance. The primary purpose of the AZO coating is electrical and the overall performance of devices is discussed in Chapter 7.

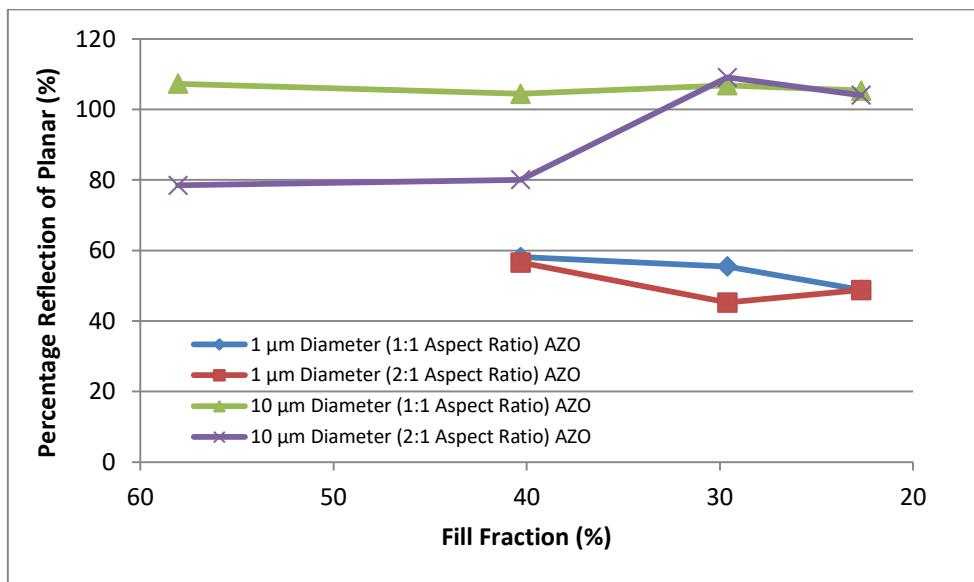


Fig 77. Percentage reflection of all AZO coated pillar samples normalised to that of an AZO coated planar sample and plotted against fill fraction of pillars

5.9. Conclusions

- The design considerations, processing and optical properties of silicon micro-pillar arrays have been described in this chapter.
- The pillar geometry and array design was informed by numerical modelling carried out in collaboration with City University. Initial modelling work indicated that low micron scale rod structures with a 50-60% packing fraction would give a reduction in reflection on the order of 40% compared to a planar silicon device. The optimal packing fraction is in agreement with that found in the literature and the predicted reduction in reflection reinforces the assertion that large scale structures can still provide useful anti-reflective properties.
- Arrays with pillar diameters in the range 1-10 μm , heights 1-20 μm and packing fractions of 20-50 % were designed for fabrication.
- The arrays were fabricated at Philips Innovation Services, Eindhoven using standard, commercial photolithographic techniques and deep reactive ion etching (DRIE). High structural quality arrays of micro-pillars were realised over 150mm diameter wafers.
- Good agreement was found between the modelled and measured reflection of the micro-pillar arrays and at the time of writing this was believed to be the first systematic study of modelled and measured arrays with identical geometry on the low-micron scale.

- Typically, at the lowest fill fraction of 40% and 1:1 diameter to height aspect ratio, arrays with 1 μm diameter pillars exhibited a 42% fall in reflection compared to planar silicon surfaces averaged over the 300-1100 nm wavelength range. For 10 μm diameter pillars, the reduction was smaller (~10%) for the same aspect ratio and fill fraction. For a given diameter, increasing pillar height or decreasing spacing (higher packing ratio) reduced reflection as expected. Comparing the reduction in reflection as a function of fill fraction to that resulting from increasing aspect ratio suggests that for relatively short pillars, aspect ratio has a greater influence than fill fraction.
- The application of AZO to both planar and pillar structured silicon samples was found to significantly reduce the measured reflection. For all samples with 40% fill fraction, AZO coated pillars typically demonstrated a 40% to 50% reduction in reflection as compared to equivalent uncoated pillars, with AZO coated planar silicon found to exhibit a similar level of improvement. As with most anti-reflective films the performance was found to vary significantly with thickness and further refinement is necessary to find an optimum thickness for both optical and electronic performance.

Chapter 6. Proximity Rapid Thermal Diffusion

This chapter will discuss the development of the proximity rapid thermal diffusion process used as a doping technique in this project. Subsequently, the efficacy of the technique will be described by presenting results for planar solar cell devices fabricated by this technique. Micro-rod cells are described in Chapter 7.

6.1. Proximity Rapid Thermal Diffusion Development

The formation of a doped emitter is a fundamental process in the production of silicon solar cells and is a well-established field. Conventional solar cell emitters are typically on the order of 1-2 µm thick and in the majority of cases are formed by diffusion of dopant impurities such as phosphorus, arsenic and boron.

Textured and structured thin silicon solar devices such as micro and nano pillar cells offer the potential for significant material savings over thick wafer and polysilicon devices but demand much tighter control of emitter parameters to prevent carrier depletion in small scale features.

Typically, emitters for structured devices are required to be highly doped and shallow. Emitters produced by spin on dopant (SOD) sources in conjunction with rapid thermal processing (RTP) permit fine control over junction depth and dopant concentration but it is a non-trivial matter to apply a conformal layer to non-uniform surfaces.

A variation on this technique, proximity rapid thermal diffusion (PRTD), sees the SOD applied to a sacrificial source wafer which is placed in proximity to samples to be doped. When heated, mass diffusion of the dopant from the SOD layer results, this is transported in the gas phase to the surface of the samples to be doped where adsorption and diffusion occurs [292].

By controlling the diffusion time and temperature it is possible to accurately control junction depths and dopant profiles whilst achieving homogeneity of doping, even on textured and structured surfaces [293].

This chapter will address the development of the rapid thermal diffusion process used to form emitters in the fabricated devices. It will also show the performance data for completed devices.

6.2. Origins of the PRTD Process

The development of the PRTD process was as a result of the unsuitability of the existing emitter formation technique at LSBU. The existing technique consisted of a grown emitter and as can be seen from the work undertaken using that technique in chapter 4 this was not a viable approach for structured devices.

It was believed that the ideal solution would be that of a diffusion doping, however this would typically require a diffusion furnace which was not available for this project. An investigation of the literature revealed various papers which reported using spin-on dopant (SOD) solutions as a gas phase diffusion doping source [294]–[299]. This took advantage of the fact that, when heated, the doping compound diffuses out of and evaporates from the source layer into the surrounding environment.

In the paper by Zagozdzon-Wosik, Grabiec and Lux, doping concentrations in the samples above 1×10^{20} atoms/cm³ with junction depths in the region of 1 μm were achieved for a diffusion time and temperature of 30 second and 1050 °C respectively.

Wang et al performed similar experiments with both phosphorus and boron based SOD solutions, this time for tunnel diodes which required very shallow junctions. The achieved doping concentrations in the range of 1×10^{21} atoms/cm³ and junction depths of 500 nm and carried out modelling which predicted the possibility of junctions as shallow as 40 nm suggesting this process as a possible solution when preparing junctions on micron scale pillars.

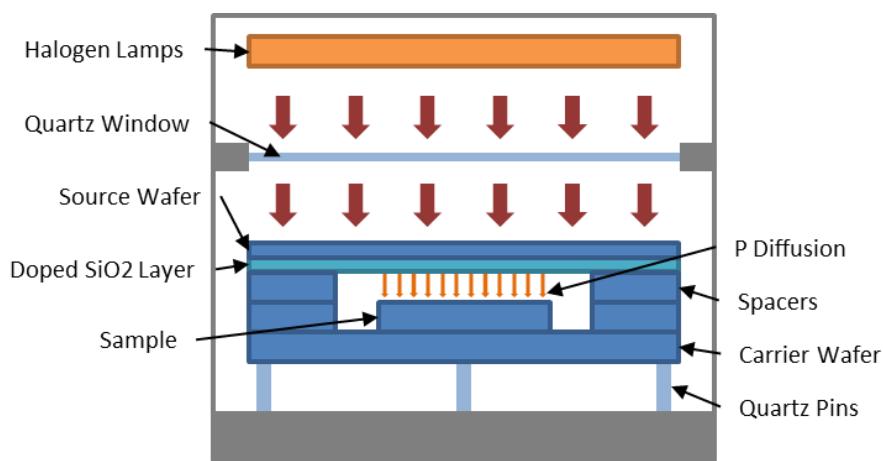


Fig 78. Equipment configuration for proximity rapid thermal diffusion. The samples to be doped are placed between a carrier wafer and the source wafer and heated resulting in dopant transport and diffusion.

A quantity of boron SOD remained from a previous project and as such a small feasibility study was undertaken to assess the basic viability of the technique for possible use in the project.

As supplied p-type <111> silicon wafers were subjected to a piranha clean process to remove organic contamination followed by de-ionised water rinse and nitrogen drying. The SOD was applied to a the wafer by spin coating and then baked at 200 °C for 30 minutes to remove residual solvent. The wafer was then placed facing n-type silicon samples to be doped in the RTP system with small pieces of silicon used to space the stack preventing contact between the source wafer and the samples (see Fig 78).

The stack was heated to 1000 °C for 60 seconds to carry out the diffusion process and then the samples were unloaded. They were then dipped in a 10% hydrofluoric acid solution to remove the glassy oxide layer which forms on the surface as a by-product of the diffusion.

Assessment of the efficacy of the process was carried out by four point probe measurements with the samples found to have a surface sheet resistance on the order of $9.69 \Omega/\square \pm 1.23$ as compared to the original wafer resistance of $\approx 30 \Omega/\square$. Application of the hot point probe method confirmed that the diffused layer was of p-type doping.

Using a variation of Fick's law [181] it is possible to approximate the depth of dopant drive in from the initial source wafer to substrate diffusion step. In the simplest form Fick's law states:

$$j = -D \frac{\partial N}{\partial x} \quad (6.1)$$

Where j is flux density (atoms/cm^2), D is the diffusion coefficient (cm^2/s), N is the concentration volume (atoms/cm^3) and x is the diffusion distance (cm). The equation can then be modified to a complementary error function:

$$C(x, t) = C_s erfc \left\{ \frac{x}{2\sqrt{Dt}} \right\} \quad (6.2)$$

Where C is the background doping concentration of the wafer being doped (atoms/cm^3), C_s is the solid solubility of the dopant (atoms/cm^3), x is the diffusion distance (cm), D is the doping element's diffusion co-efficient (cm^2/s), and t is the diffusion time (s).

The background doping (C) of the p-type wafer is $9.67 \times 10^{15} \text{ atoms}/\text{cm}^3$ and at 1000°C the boron saturation concentration (C_s) is $3.5 \times 10^{20} \text{ atoms}/\text{cm}^3$ [300]. The complementary error function can then be re-arranged to describe the diffusion behaviour:

$$\operatorname{erfc}\left\{\frac{x}{2\sqrt{Dt}}\right\} = \frac{9.67 \times 10^{15}}{3.5 \times 10^{20}} = 2.76 \times 10^{-5} \quad (6.3)$$

Referring to the erfc function plot (shown on page 46, chapter 3) relating normalised concentration versus normalised distance gives:

$$\text{For } \frac{C}{C_s} = 2.76 \times 10^{-5}, \quad \frac{x}{2\sqrt{Dt}} = 3.1 \quad (6.4)$$

By re-arranging the second equation above to make the diffusion depth (x) the subject:

$$x = 3.1 \times 2\sqrt{Dt} \quad (6.5)$$

and substituting the boron diffusion co-efficient (D) at 1000 °C of 5×10^{-14} cm²/s [175] and the diffusion time (t) of 60 seconds, it can be shown:

$$x = 3.1 \times 2 \times \sqrt{(5 \times 10^{-14})(60)} = 1.04 \times 10^{-5} \text{ cm or } 0.104 \mu\text{m} \quad (6.6)$$

To confirm experimentally the dopant diffusion depth, an etch process of known etch rate was used to remove thin layers from the sample with a measurement of sheet resistance taken between each etch cycle. This was repeated until the measured value matched that of the wafer prior to doping indicating that the entire doped layer had been removed.

The etch used consisted of Hydrofluoric (HF), Nitric (HNO₃) and Acetic (CH₃COOH) acids commonly referred to as HNA etch. The Nitric acid is a strong oxidiser which converts the silicon to silicon oxide which is then etched by the hydrofluoric acid. The Acetic acid acts as a buffer to stabilise and control the etch rate. The 1:20:4 - HF : HNO₃ : CH₃COOH solution used gave a stable etch rate of 360 nm/min which allowed for 5 second etches at 30 nm per etch. After each etch the samples were thoroughly rinsed in deionised water and the sheet resistance measured by four point probe.

Fig 79 shows the measured sheet resistance as a function of etch depth. It is apparent that around the 200 nm mark the doping concentration has returned to that of the substrate wafer sample. This suggests that there is an inaccuracy in the calculated initial diffusion depth of ≈ 100 nm. Considering the variables, the only value which could cause a discrepancy so readily is the boron diffusion co-efficient which itself is based on process temperature.

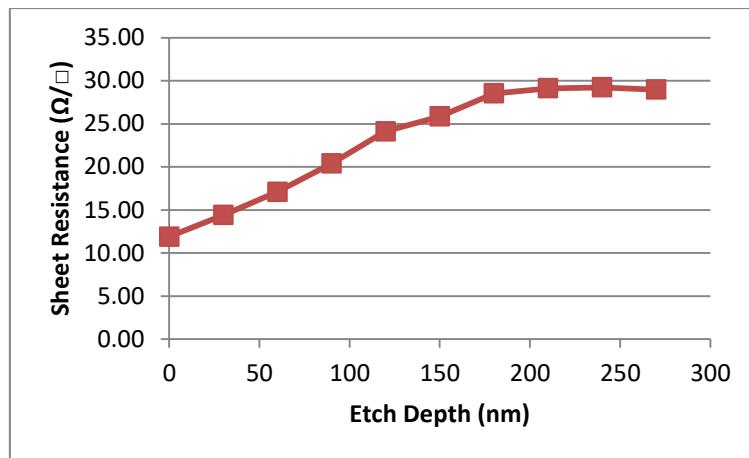


Fig 79. Change in sheet resistance as a function of etch depth of diffused sample

Fig 80 demonstrates the effect of temperature change on the final calculated diffusion depth with all other variables isolated.

It is apparent that a relatively minor discrepancy would be capable of increasing the diffusion rate to the extent that a diffused junction would reach 200nm. It was theorised that this discrepancy might be as a result of the configuration of the temperature measurement arrangement of the RTP system during the diffusion process.

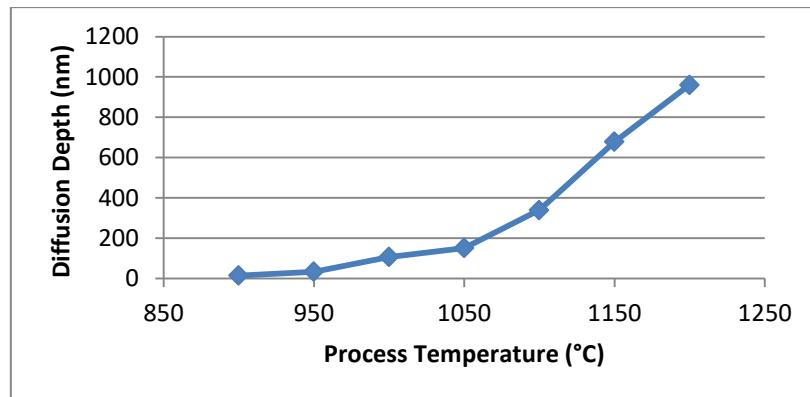


Fig 80. Calculated diffusion depth of boron in silicon wafer as a function of process temperature for a 60 second proximity rapid thermal diffusion step

Under normal configuration the RTP system uses a pyrometer to read the temperature off the backside of a wafer directly exposed to the lamp array. However, under the diffusion arrangement, an additional wafer and an air gap is introduced which affects the thermal propagation of the system. The effect of this was tested experimentally by the following method.

The RTP was configured with a spaced wafer stack as per a diffusion run and the temperature ramped to 1000 °C as measured by the system pyrometer. Once stabilised the output power required was noted (600%) and the system allowed to cool. The top wafer was removed and the system set to the previous output power. The resulting temperature was then noted and found to be on the order of 1065-1072 °C suggesting that the temperature in the middle of the stack during diffusion is somewhat higher than the set 1000 °C. This excess temperature would effectively account for the greater diffusion depth than calculated.

Fig 81 is extracted from the data for a test solar cell which was produced from a sample diffused with boron. A gold layer was sputtered onto the rear to act as a back contact and a small amount of silver paint used on the front to give a spot contact. Whilst not optimised contacts, Suns-V_{oc} does not rely on current extract and therefore the resistivity of the contacts is not of major concern.

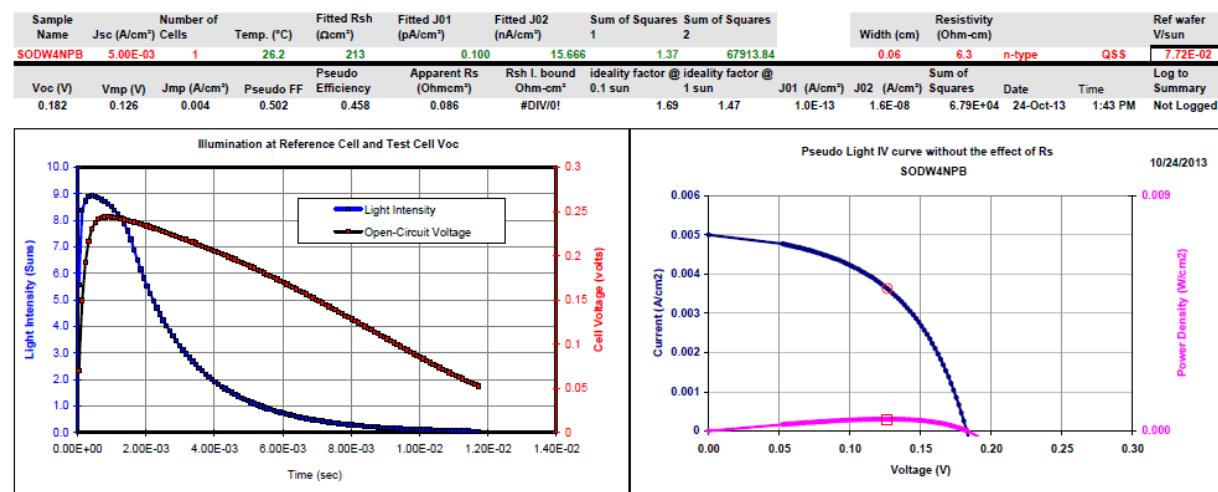


Fig 81. Extract of Suns-V_{oc} data for n-type wafer with p-type diffused junction

It is evident from the low measured open circuit voltage (V_{oc}) of 0.182 V and the very low value for current at maximum power (J_{mp}) of 0.004 A/cm² that the device would be ineffective as a solar cell based on this diffusion process. Additionally, the dopant utilised is p-type in this case and is required to be n-type for the structured devices. However, as an indicator of the ability to prepare a junction via proximity rapid thermal annealing with the available in-house equipment, it demonstrated the necessary proof of concept.

6.3. Phosphorus PRTD - SOD Source and Equipment Configuration

As the initial proof of concept of PRTD as a means to fabricate emitters had been proven with p-type boron based SOD, it was necessary to develop and refine the process for an n-type phosphorus based solution.

As supplied p-type <111> silicon wafers were subjected to a piranha clean process to remove organic contamination followed by de-ionised water rinse and nitrogen drying.

The SOD solution (supplied by Filmtronics) consisted of phosphorus pentoxide (P_2O_5) and silicon dioxide (SiO_2) in a solvent carrier. The SOD was applied to the wafer by pipette which was then spun at 1000 rpm for 30 seconds to produce a uniform film. The wafer was then baked at 200 °C for 30 minutes to drive off residual solvent and leave a P_2O_5 containing SiO_2 film on the surface. When necessary the SOD solution was diluted with Methanol (CH_3OH) to vary the phosphorus concentration.

Samples to be diffused were prepared from 675 µm thick <100> silicon wafers with resistivity of 0.1-0.5 Ω cm cleaved into 13 mm² samples. Prior to processing they were subjected to a piranha etch process, de-ionised water rinse process and N₂ drying. These were then loaded into the RTP system on top of a silicon carrier wafer. Spacers consisting of pieces of silicon wafer were placed around the edge of the carrier before the source wafer was placed atop these to complete the diffusion stack.

After loading, samples were subjected to a variety of diffusion processes with temperature varied in the range 770 °C – 1030 °C and oxygen (O₂) content in the nitrogen (N₂) process gas varied in the range 0-10% (50-400 sccm). The addition of oxygen to the diffusion atmosphere removed the requirement of the evaporated P_2O_5 diffusant to act as an oxygen source. This was found to improve the uniformity of dopant incorporation into diffused emitters and as a result improved the average performance of devices.

Typical thermal cycles for diffusions consisted of a fast ramp (< 60 s) to the peak diffusion temperature followed by a hold period. At the end of the hold the temperature was ramped down to 500 °C over a short period (≈180 s) to improve reorganisation of the diffused phosphorous in the silicon lattice and reduce defects.

6.4. Diffusion Uniformity

It was noted early on that significant variation could occur in both the sheet resistance of a diffused emitter on a single sample and the uniformity of the sheet resistance across multiple samples from the same diffusion run.

To assess the cause and extent of this non-uniformity an experiment was devised to “map” the dopant diffusion occurring in the chamber of the RTP system during a typical diffusion process. Twelve 18 mm x 13 mm samples were prepared using the normal acetone clean and piranha etch process and then arranged around on the carrier wafer as per Fig 82.

A 970 °C diffusion cycle was then run for 15 minutes to form an emitter on the arrayed samples. Post diffusion the samples were removed from the chamber and dipped in a 5% HF acid solution to remove the residual SiO₂ layer from the surface. The surface sheet resistance of each sample was then mapped using a four point probe station to create a 5 x 4 grid of measurements.

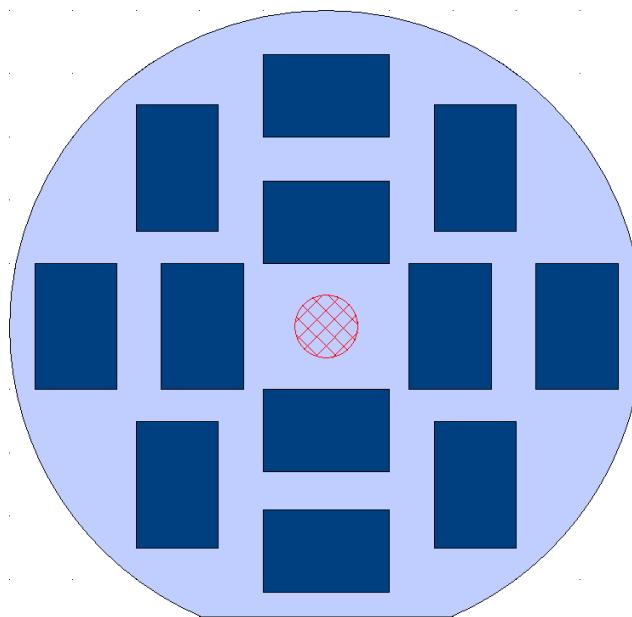


Fig 82. Wafer Layout for uniformity experimentation

By arraying these measurements in a graphical fashion with the same layout as the samples in the RTP system it is possible to view the diffusion uniformity visually.

It was found that uniformity became steadily worse for samples placed at increasing distances from the centre point of the carrier wafer. Due to the relatively small temperature variation from the centre to the outer edge it was not deemed plausible that this could be responsible for the non-uniformity. The other major factor likely to affect the uniformity of doping is the process gas which is responsible for the mass transport of the volatile dopant compounds from the source wafer to the samples to be doped.

As the gas flow rate could not be substantially reduced for reasons that are explained later in this chapter, it was decided that the solution to the uniformity issue was to limit sample positioning to the green area shown in Fig 83. This region was found to have a standard deviation of 4.8 versus 37.3 for the whole diffusion area which was felt to be adequately uniform for the purposes of this work.

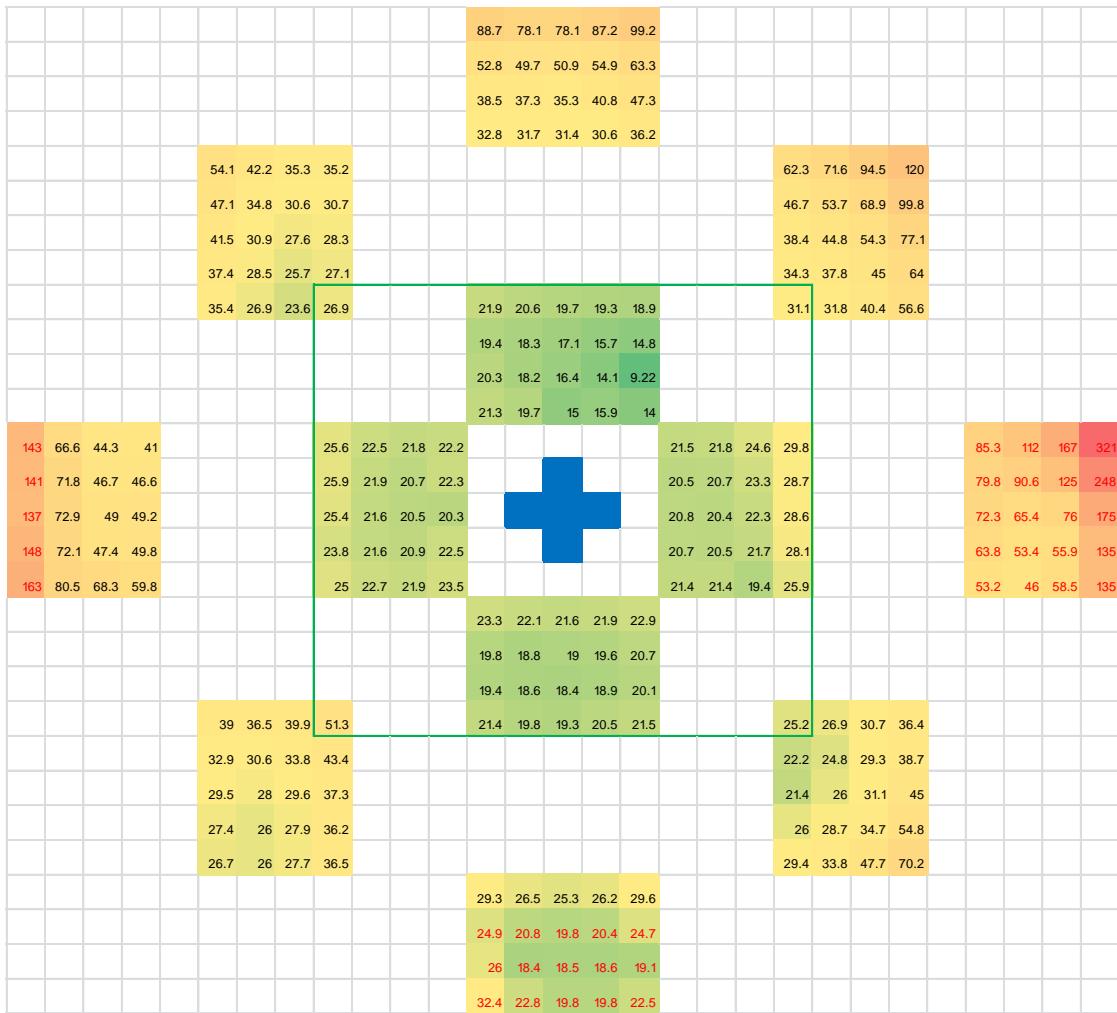


Fig 83. RTP Diffusion Uniformity Mapping with sheet resistance values in Ω/\square . Values in red are for sample areas that either came into contact with the source wafer, resulting in very low values or samples that were knocked out of the diffusion zone with resulting high values

6.5. SOD Concentration and Process Gases

The SOD solution utilised for the PRTD process was supplied with a 4% concentration of the P_2O_5 dopant compound. To assess the effect of varying this concentration, the solution was “cut” with methanol and applied by spin coating to a sacrificial source wafer and a diffusion process run. From this point onward, dopant concentration will be referred to as percentage of original, i.e. 100% is as supplied 4% solution, 50% is 2% and so forth.

All diffusions were carried out at 870 °C for 15 minutes in a flowing 200 sccm nitrogen process atmosphere. The thickness of grown oxide and the sheet resistance of the diffused layer were measured by ellipsometry and four point probe respectively (Fig 84). Note that the error bars shown for sheet resistance across all graphs indicate the standard deviation of multiple surface measurements and give an indication of the diffusion uniformity.

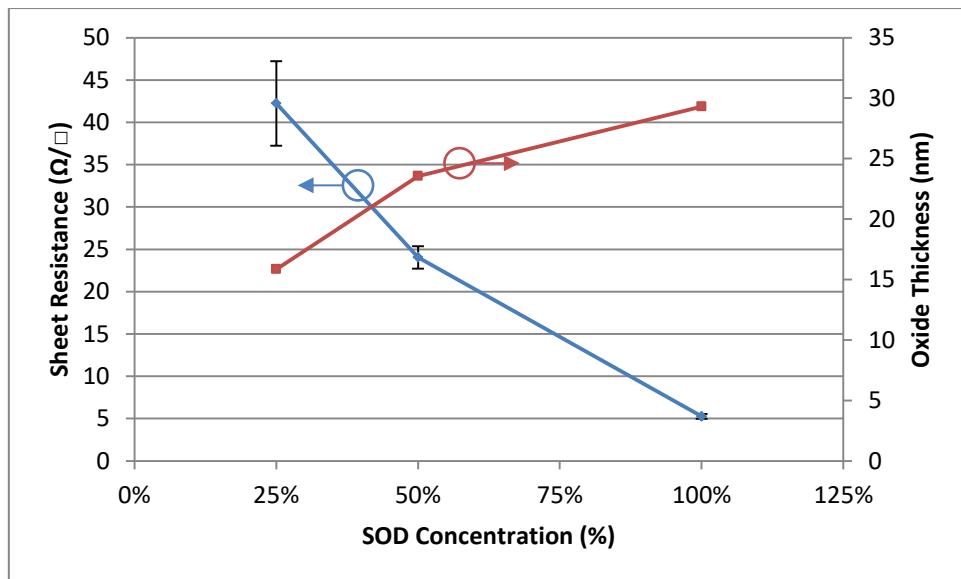


Fig 84. Effect of SOD concentration on diffused emitter sheet resistance and grown oxide thickness

Reducing the P_2O_5 availability has a dual effect on the diffusion process as it is responsible for supplying not only the phosphorus impurity but also the oxygen which forms the SiO_2 on the silicon surface according to the reaction:



The resulting effect of reduction in SOD concentration is increasing sheet resistance and reduced surface oxide thickness. An increase in the standard deviation of the sheet resistance measurements was also noted on diffused samples indicating poorer diffusion uniformity. It is believed that this results from the low concentration of P_2O_5 in a flowing N_2 atmosphere resulting in inconsistent adsorption onto the surface of the samples to be doped.

This was further assessed by selecting a 50% solution and repeating the previous diffusion parameters with differing N_2 flow rates. As previously, the thickness of grown oxide and the sheet resistance of the diffused layer were measured by ellipsometry and four point probe respectively (Fig 85).

Whilst the variation in sheet resistance between 200 sccm and 400 sccm is not significant, there is a tenfold increase in the standard deviation of the surface sheet resistance measurements. Increasing the gas flow substantially results in a much more significant increase in the average surface sheet resistance and a further increase in the standard deviation. This suggests that at the high N_2 flow rate a meaningful proportion of the P_2O_5 that is subliming from the carrier wafer is being transported straight through the RTP system

either without coming into contact with the doping samples or without being efficiently adsorbed at their surface's. It is apparent, however, that the diffusion process is still occurring as despite the poor uniformity the diffused samples still exhibit identifiably n-type diffusion. A lack of surface adsorption is further supported by the reduction in grown oxide thickness measured on the diffused samples.

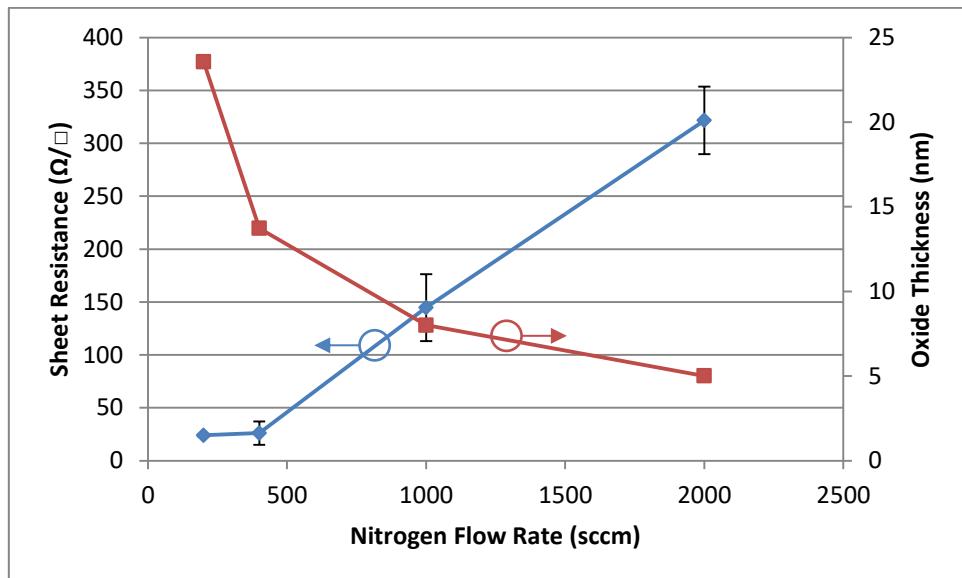


Fig 85. Effect of nitrogen flow rate on diffused emitter sheet resistance and grown oxide thickness

It was also necessary to establish the continuing efficacy of diffusion at high N₂ flow rates as another factor to be investigated was the addition of oxygen (O₂) to the diffusion atmosphere. Due to the lower operable limit of each mass flow controller (MFC) on the RTP system being 40 sccm it was necessary to be able to flow at least 1600 sccm of N₂ to allow a 2.5% O₂ in N₂ gas mixture to be achieved. By attaining diffusion at 2000 sccm it was therefore possible to achieve the minimum required 2.5% O₂ in N₂ using 50 sccm of O₂. Whilst the MFC would theoretically operate at 40 sccm, it had proven to be unstable at this setting, making the ability to run at 10 sccm higher useful.

It had been proposed that the addition of oxygen to the process atmosphere would enhance the diffusion rate of phosphorus into the silicon. This was based on the principle that phosphorus diffuses in silicon by interstitial vacancy diffusion and that interstitial vacancy generation is enhanced in the presence of a growing oxide.

To assess the effect of O₂ in the process atmosphere on the diffusion process a series of diffusions were run with increasing percentages of O₂ in N₂. All diffusions were undertaken at 870 °C for 15 minutes under 2000 sccm of N₂ with O₂ varied in the range 2.5% to 20%. As in

previous cases, the thickness of grown oxide and the sheet resistance of the diffused layer were measured by ellipsometry and four point probe respectively (Fig 86).

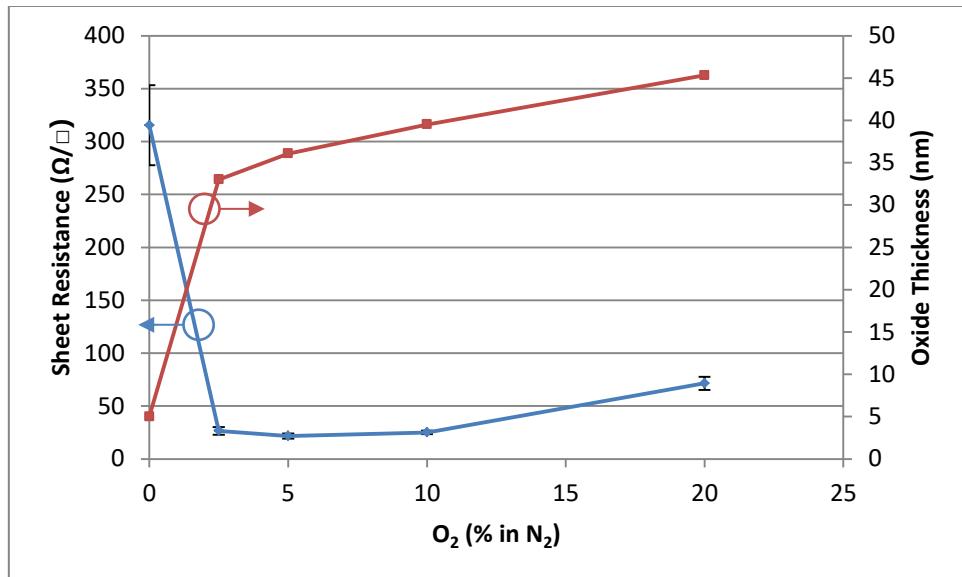


Fig 86. Effect of oxygen in process atmosphere on diffused emitter sheet resistance and grown oxide thickness

The effect of adding O_2 to the N_2 atmosphere is significant with both a tenfold reduction in the sheet resistance and a sevenfold increase in the grown oxide thickness on the diffused samples for a 2.5% O_2 in N_2 mixture. The addition of further O_2 up to 10% in N_2 has a minimal effect on the sheet resistance of diffused samples but does result in further improvements in the uniformity. The grown oxide thickness also increases steadily with additional O_2 up to 10% O_2 in N_2 .

The effect of oxygen on uniformity can be better highlighted by comparing the sheet resistance maps of samples taken from each run (shown in Fig 87).

The effect of adding any amount of oxygen on uniformity is immediately apparent with smaller but still visible improvements with further additions up to 10% O_2 in N_2 . The addition of excess O_2 to the diffusion atmosphere modifies the diffusion mechanism occurring at the surface of the silicon. In a pure N_2 atmosphere the disassociation of the P_2O_5 occurs predominantly at the silicon surface with the phosphorus diffusing directly into the silicon and the oxide forming on the surface. With a surplus of oxygen, the oxide layer grows on the surface more rapidly and the phosphorus is incorporated into the oxide forming a phosphosilicate glass. This glassy layer then becomes the impurity source with phosphorus atoms continuing to diffuse from this layer into the silicon.

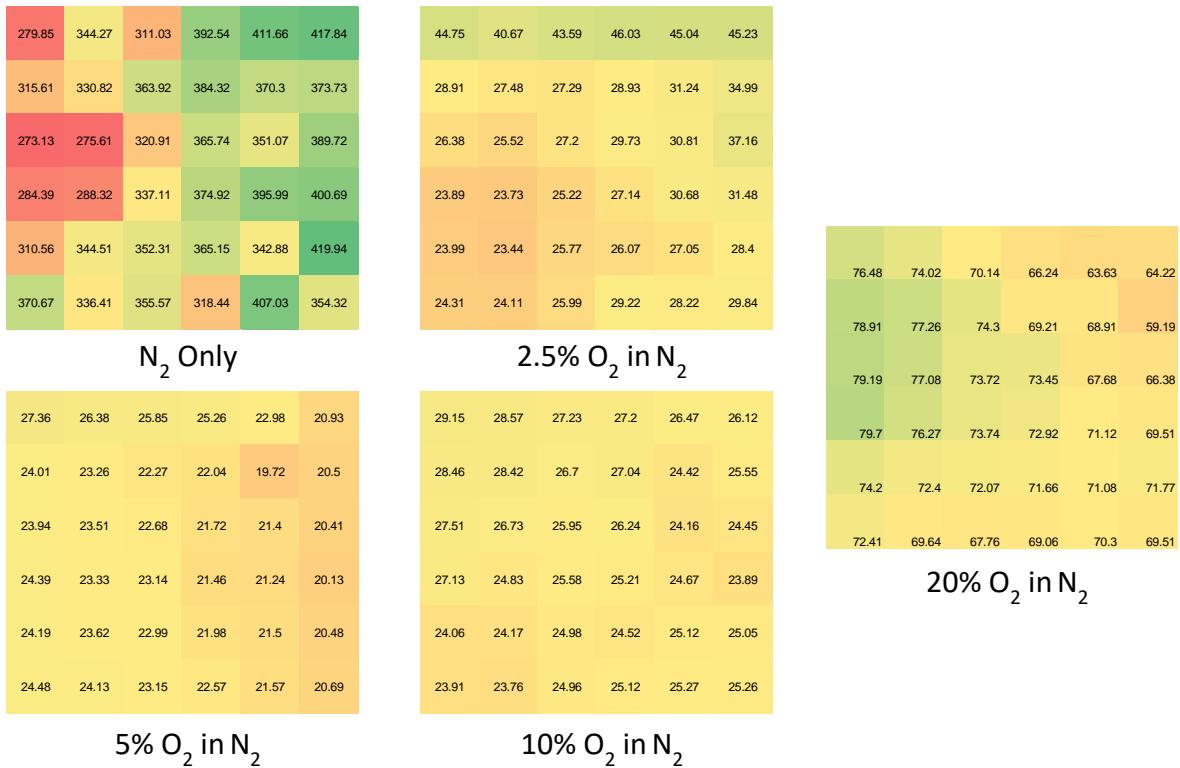


Fig 87. Effect of oxygen concentration on sheet resistance uniformity

At 20% O₂ in N₂ there is a marked decrease in the grown oxide thickness coupled with a rise in sheet resistance from an average of 25 Ω/□ to over 70 Ω/□. The increasing O₂ concentration leads to competitive surface reactions, with SiO₂ growth occurring more rapidly than phosphorus can be incorporated into the phosphosilicate glass and reducing the amount of dopant available to the silicon surface. This leads to a lower doping concentration and a rise in sheet resistance despite adequate dopant being available in the diffusion atmosphere.

Notably, the thickness of oxide formed at the diffusion temperatures under investigation does not agree with conventional oxide growth theory. However, oxide formation by RTP has been shown to yield much higher oxidation rates compared to conventional furnaces [185]. The enhanced oxide formation may also account for the deep junctions and high peak doping concentrations achieved (discussed in the follow section) at relatively low temperatures, which do not agree with conventional diffusion theory. It has been shown that phosphorus diffusivity is significantly enhanced in the presence of a growing oxide. This is believed to be due to the enhanced silicon self-interstitial formation under oxidation conditions and an associated increase in interstitial dopant diffusion, the primary means of phosphorus transport in silicon, which results [301].

6.6. Process Temperature

The effect of diffusion temperature on sheet resistance and junction depth is plotted in Fig 88. Due to hardware limitations, the diffusion undertaken at 1030 °C was limited to 10 minutes rather than the 15 minutes utilised for the lower temperature processes. By calculating the diffusion rate and correcting for the shorter run time an approximation for the 15 minute junction depth is plotted (shown by hashed line). Applying an exponential fit, as expected for diffusion rate vs temperature, to the corrected curve gives an acceptable fit lending confidence to the correction.

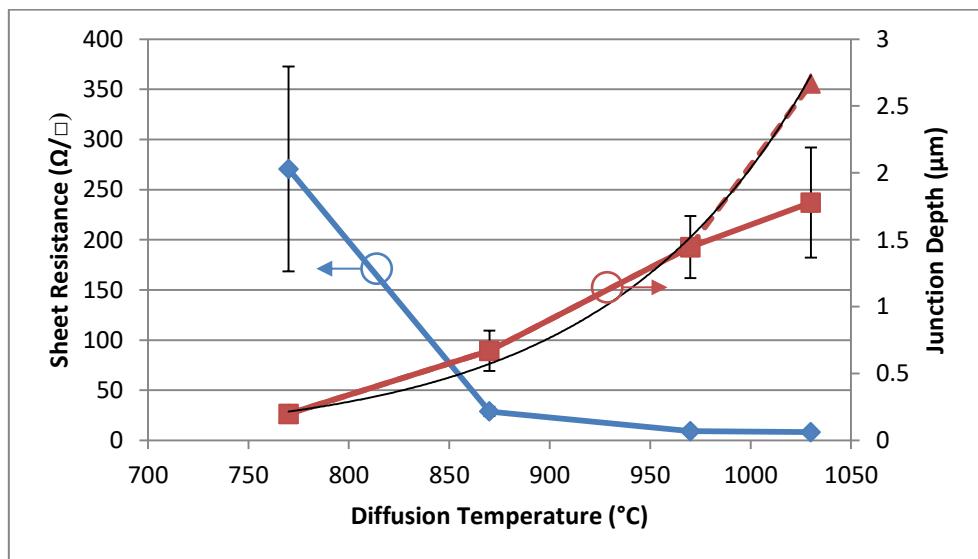


Fig 88. Sheet resistance and junction depth vs diffusion temperature

There is a significant decrease in sheet resistance between 770 °C and 870 °C. By calculating an average value for emitter resistivity based on the sheet resistance and the measured junction depth it is possible to use the calculated ERFC plots shown in Fig 89 to estimate the peak surface concentration. The limitation of this technique is that it relies on sheet resistivity which is a function of sheet resistance and sheet thickness. Additionally, it assumes that the film has a uniform doping concentration which will not be the case for a diffused, rather than grown, emitter. The approximated values, therefore, are likely to be generally appropriate for the doping concentration at the front surface of the device but will not be representative of the doping throughout the bulk of the emitter.

At 770 °C a peak concentration of 6×10^{19} atoms/cm³ is approximated, rising to 1×10^{20} atoms/cm³ at 870 °C. This substantial increase effectively explains the significant fall in sheet resistance.

A smaller increase from 1×10^{20} atoms/cm³ to 3×10^{20} atoms/cm³ between 870 °C and 970 °C occurs as the electronically active limit of phosphorus in silicon

($\approx 3 \times 10^{20}$ atoms/cm³) is approached [175]. Above 970 °C there is little change in the sheet resistance despite a large increase in junction depth. Whilst the solid solubility of phosphorus in silicon increases above 970 °C (rising to a peak slightly greater than 1×10^{21} atoms/cm³ at 1100°C) it cannot be effectively measured electronically as above 3×10^{20} atoms/cm³ none of the additional donor carriers are electronically active and able to increase conduction.

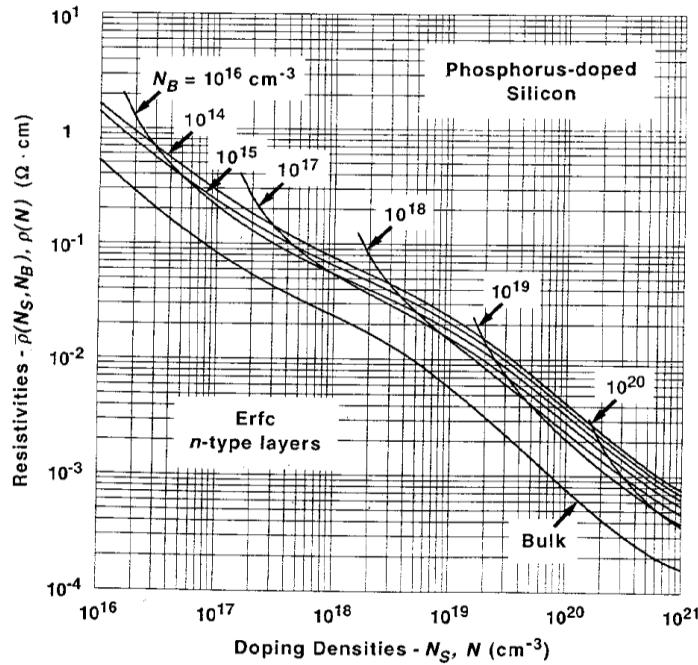


Fig 89. Calculated ERFC Plots for Various Background Doping Densities vs Measured Resistivity [175]

Whilst the increase in dopant concentration above 970 °C is not measureable, or arguably relevant from a device point of view, an increase in temperature also serves to increase the diffusion rate of the phosphorus in silicon. This is in agreement with the results shown in Fig 88 with a significant increase in junction depth for a temperature increase from 970 °C to 1030 °C.

Establishing that the available level of dopant exceeds the solid solubility of phosphorus in silicon is important as it means it is reasonable to make assumptions about the diffusion process based on the unlimited source diffusion model. It also confirms that by maintaining a high diffusion temperature, but reducing diffusion time, it should be possible to retain a high peak doping level but with reduced junction depth which will be crucial for pillar device emitter formation.

6.7. Effect of Emitter Thickness on Device Performance

The majority of the development of the PRTD process to this point was aimed at gaining control of doping level and uniformity. As the maintained variable was the diffusion time the

junction depth (x_j) increased significantly for each increase in diffusion temperature. To study the effect of emitter thickness of device performance, devices on unstructured, planar Si wafers were fabricated using the PRTD process. The device fabrication steps are highlighted in Fig 90.

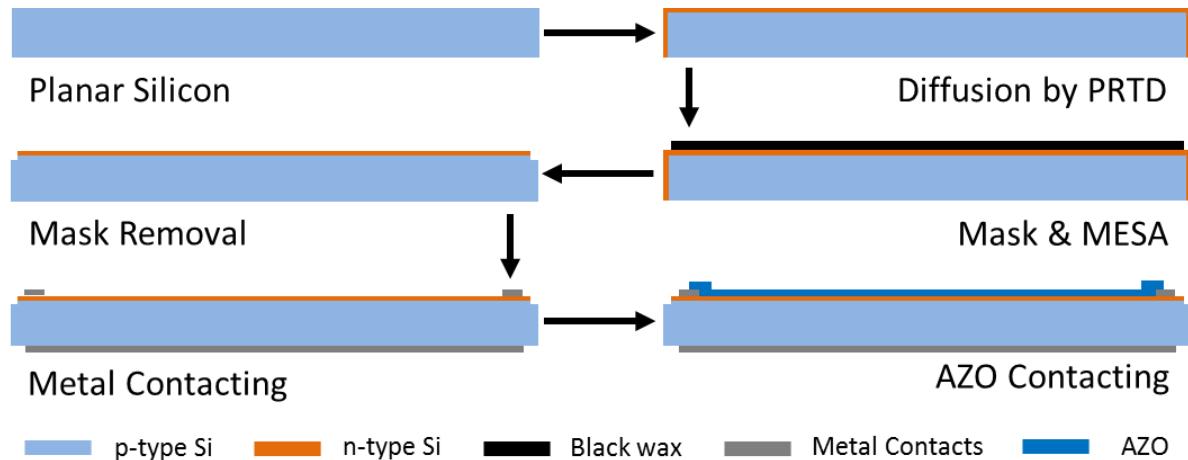


Fig 90. Fabrication steps for a planar silicon PV device with emitter formed by PRTD. The mask used for the MESA process is black wax. The rear metal contact is sputtered aluminium whilst the front contacts are bi-layer nickel/silver. The AZO contact is prepared by sputtering and prevented from wrapping around the device by a foil mask.

Samples were first cleaned in an ultrasonicated acetone bath for five minutes followed by rinsing in running de-ionised water and then nitrogen blow dried. After this initial clean step the samples were subjected to a 20 minute piranha etch. Samples were then transferred to a de-ionised water rinse for 10 minutes before further rinsing in flowing de-ionised water and a nitrogen blow dry.

At this point the samples were prepared to the necessary standard for diffusion and were loaded to the RTP system for the PRTD process. The diffusions were undertaken at varying temperatures using a 50% SOD concentration source wafer in a flowing 10% O₂ in N₂ process environment.

After diffusion the devices required MESA edge isolation to prevent shunting caused by wrapping of the junction resulting from the gas phase diffusion process. In industry this is typically carried out using plasma etching, however, this approach was not available in this instance. An alternative to plasma etching is wet etching, which demands less equipment and provided very high levels of accuracy are not required, is a more straightforward process.

As mentioned in section 4.5.2. the wet etch selected for the MESA process was an HNA solution consisting of a 1:1:2 ratio of hydrofluoric acid, nitric acid and acetic acid. Due to the aggressive nature of the etch and the inability to effectively deposit conventional hard mask layers (metal or SiN) it was necessary to select an alternative masking material. This led to the development of the “black wax” technique which was ultimately used. Black wax is a common name for Apezion Wax W which was originally developed as a sealant for vacuum systems. It is a hydrocarbon based wax which is exceptionally resistant to a wide range of aggressive etches including HNA but is conveniently broken down by a range of aromatic hydrocarbons or organochlorides. Additionally, despite not being an intended benefit, black wax has good gettering properties, trapping impurities which are removed with the wax.

The black wax has a low softening point (≈ 90 °C) permitting straightforward fabrication of appropriately shaped masking pieces by forming the wax in a mould prior to application. The moulded pieces are then adhered to the samples by heating the samples on a hot plate and allowing the black wax to reflow before rapid cooling on a cold plate to set the mask.

After masking the samples were first dipped in a 50% HF solution to strip the residual SiO_2 from the diffusion process which could result in uneven MESA etching as SiO_2 is itself an etch mask. Subsequently the samples were subjected to a 60 second etch in the HNA solution followed by a 5 minute rinse in de-ionised water. They were subsequently re-rinsed in flowing de-ionised water and nitrogen blow dried. In addition to the edge isolation on the front surface, the etch process also removes any n-doped regions on the rear side resulting from wrap-around diffusion.

Removal of the black wax was achieved using toluene in an ultrasonic bath to expedite the mask breakdown. On removal from the toluene, which was now saturated with black wax, the rapid evaporation of the solvent left a thin residue on the surface of each sample. This was removed in a fresh batch of ultrasonicated toluene to leave a near perfectly clean sample surface. Finally all samples were dipped in a further fresh batch of toluene as a polishing process to ensure total removal of black wax. Samples were then rinsed in flowing de-ionised water to remove any residual toluene followed by a nitrogen blow dry.

After MESA etching and mask removal the residual SiO_2 from under the mask was still outstanding and required a further dip in a 50% HF solution, followed by de-ionised water rinse and nitrogen blow dry.

The aluminium back contact is applied by sputter deposition and requires a mask to prevent contact wrap-around. As the mask must be conductive to prevent charging effects affecting

the sputter process, vacuum grade aluminium foil with the necessary sized aperture cut in it was selected and applied to the sample by wrapping.

After deposition the masking was removed and the devices were loaded to the RTP system for annealing to form an ohmic contact. Post annealing and prior to depositing the front metallised contact it was necessary to remove the native oxide that had reformed in the interval following the previous HF dip. Despite being only on the order of a few nanometres thick, it was found by experimentation that it was crucial to remove this oxide otherwise the front silicide based contact is Schottky rather than ohmic. Due to the incompatibility of the aluminium back contact and HF and to remove the necessity for re-masking, the sample was oxide stripped in a shallow bath of HF that only came into contact with the front surface.

The sample was affixed to a stainless steel mask with openings for 1.5mm dot contacts and a bi-layer nickel/silver stack was deposited by vacuum thermal evaporation. Post deposition the devices were loaded to the tube furnace for a 15 minute anneal at 420 °C to form the nickel silicide interface. These metal contacts allowed effective I-V characterisation of the devices prior to application of the transparent conductive oxide in the following step to assess the effect of the TCO on various device parameters.

The final processing step involved a further HF etch to once again remove the native silicon oxide before a sputter deposited layer of aluminium zinc oxide was applied to the front surface of the device to reduce series resistance and improve current collection. Like the aluminium back contact, the TCO was deposited through a vacuum grade aluminium mask to prevent contact wrap-around. The resulting front surface arrangement is illustrated in Fig 91.

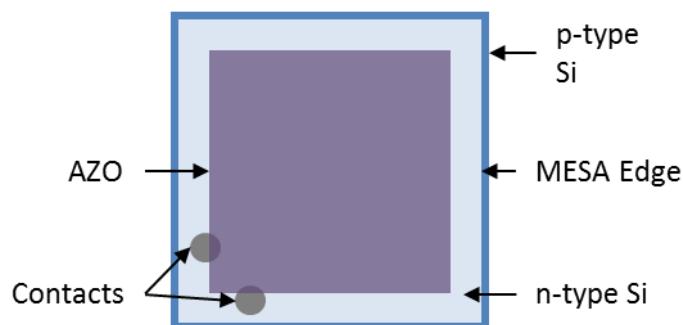


Fig 91. Top contact arrangement on PRTD diffused cells.

Devices to be characterised were mounted on a thermal stage to maintain the required temperature of 25 °C, whilst a vacuum chuck ensured good contact with the rear side metallisation. The samples were shadow masked so that only the active area (81 mm^2) was

illuminated and a sprung contact probe contacted the top contact and consequently the transparent conductive oxide layer.

The effect of increasing emitter depth (resulting from increased diffusion temperature) on device performance is illustrated by the current density (J)-voltage (V) data of Fig 92(a). The diffusion time in each case was the same at 15 minutes. Table 7 presents the device parameters extracted from this data. Fill factor can be observed to rise with increasing emitter thickness and doping concentration suggesting an improvement in charge separation. Additionally, shunt resistance rises and series resistance falls with increasing junction depth due to the reduction in potential shunt paths and lower emitter sheet resistance, respectively. The thinnest emitter exhibits the highest sheet resistance as expected, leading to the poor shape of the J-V curve.

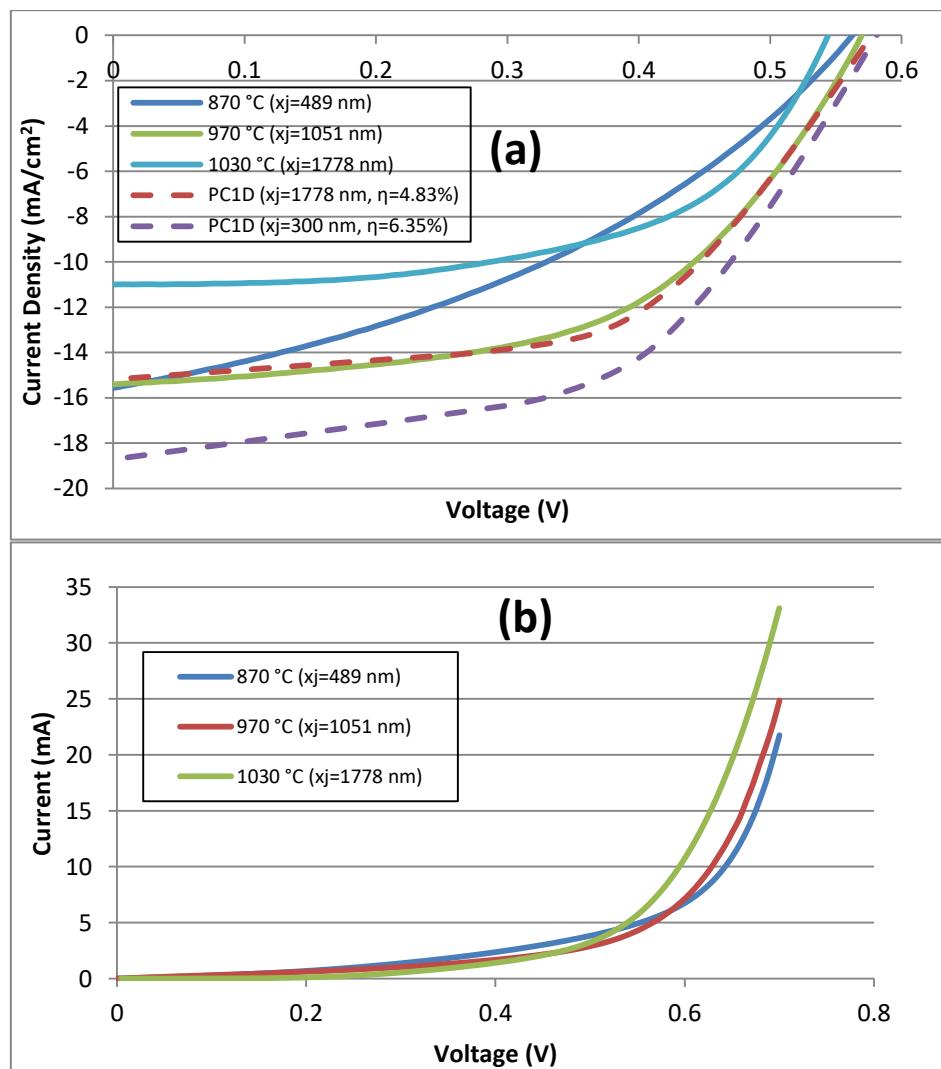


Fig 92(a). Light I-V and **(b)** Dark I-V curves highlighting the effect of varying junction depth caused by different diffusion temperature on device performance plus associated PC1D modelling

Furthermore, whilst typical planar solar emitters are on the order of $< 1 \mu\text{m}$ thick, they would typically have a peak surface dopant concentration greater than $1 \times 10^{18} \text{ atoms/cm}^3$. The emitters under development here have typical surface concentrations greater than $1 \times 10^{20} \text{ atoms/cm}^3$ which at conventional emitter thickness would result in significant performance losses. This results because at doping concentrations of this level there is a very high concentration of defects in this region, leading to very short carrier lifetimes so carriers recombine rapidly before they can be collected. As a result, a majority of the light that is absorbed in this region will not result in photocurrent generation. This could explain why the thickest emitter in Fig 92(a) (1030°C) has the lowest short circuit current density although it demonstrates a good I-V response. The dark I-V characteristics of Fig 92(b) below $\approx 0.5 \text{ V}$ are consistent with the Fill Factor (FF) and Shunt Resistance (Rsh) values reported in Table 7. As expected the leakage across the junction improves with increasing junction depth resulting in the improving fill factor and due, in part at least, to the rising shunt resistance.

Junction Depth (nm)	489	1051	1778
Voc (V)	0.56	0.57	0.54
Jsc (mA/cm^2)	13.21	15.40	9.33
Fill Factor (%)	37.73	53.73	56.90
Rsh ($\Omega \text{ cm}^2$)	117	370	1490
Rs ($\Omega \text{ cm}^2$)	17.20	10.90	9.61
Efficiency (%)	3.43	4.89	3.53

Table 7. Performance parameters for devices with emitter thickness varied by diffusion temperature

It has been shown in the literature that it is possible using PRTD to achieve shallow diffusion of phosphorus whilst maintaining the necessary high dopant concentration required for efficient thin emitters. As demonstrated thus far, the high dopant levels are clearly achievable; however, they must continue to be attainable for shorter diffusion cycles to permit thinner emitters to be fabricated.

To investigate the theoretical performance gains that might be achievable with thin, highly doped emitters, a PC1D model was developed based on parameters extracted from a real device fabricated by a 15 minute, 970°C diffusion. The parameters for the model were refined until a good fit to the real device I-V curve was achieved. The comparison between the modelled and measured curve is shown in Fig 92(a) by the red hashed line and solid green line respectively. Once this fit was achieved, the PC1D model emitter thickness

parameter was reduced in steps to find the likely levels of improvement which might be achievable.

The predicted efficiency versus junction depth is plotted in Fig 93. It suggests a steady improvement by reducing the junction depth to 300 nm followed by a plateau at just over 6%. The resulting predicted I-V curve is shown in Fig 92(a) by the hashed purple plot. Further reductions in junction depth down to 5 nm resulted in a predicted efficiency improvement of only 0.07% but an increase in emitter sheet resistance of nearly $2500 \Omega/\square$. As the emitter must carry the light generated current, albeit only as far as the nearest contact, it is preferable that the emitter possess as low an emitter sheet resistance as possible. It was decided therefore that as a 300 nm emitter was adequately shallow to be applicable to 1 μm pillar devices and there was little improvement to be gained by reducing the depth further that this should be a target depth for further PRTD junction development.

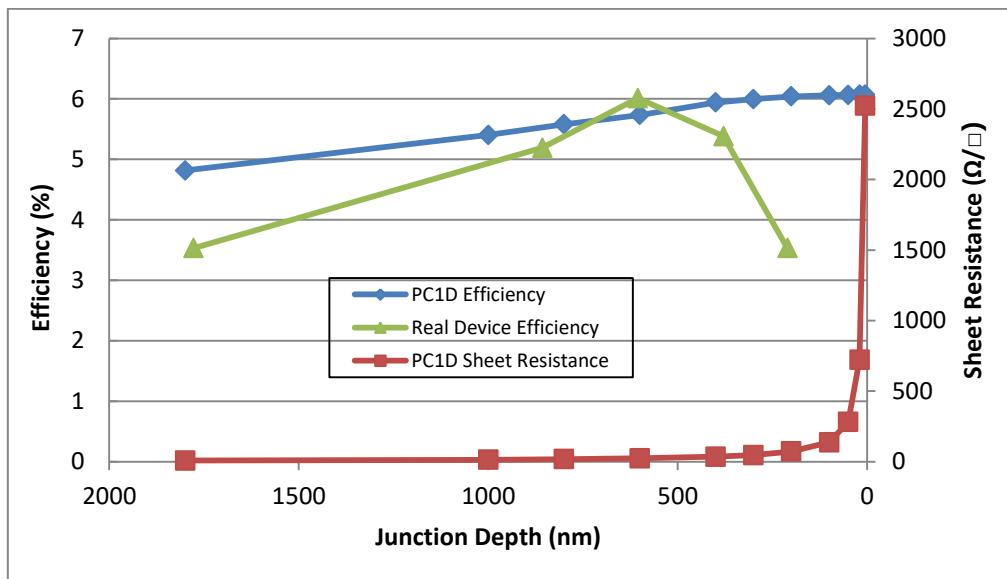


Fig 93. Effect of emitter thickness on device efficiency and sheet resistance

With a target junction depth established it was necessary to find the PRTD parameters that would achieve this requirement. For conventional diffusion processes it is possible to achieve a good approximation of the required diffusion parameters through variations of Fick's laws of diffusion. However, because the PRTD process is affected by multiple variables; source out-diffusion rate, mass diffusion rate, adsorption rate and the effect of oxide growth on the diffusion rate, it would be difficult to predict such a shallow junction depth mathematically with meaningful accuracy. Instead, the parameters were assessed experimentally with successive diffusion runs undertaken at 1030 °C with progressively shorter diffusion periods. This higher value than the modelled 970 °C was selected as

devices diffused at this temperature exhibited superior fill factor than those diffused at the lower values.

The depths of the resulting diffusions were monitored by ball grooving and staining (results in Table 8) and devices were fabricated from each diffusion run to establish the effect of junction depth on electronic performance.

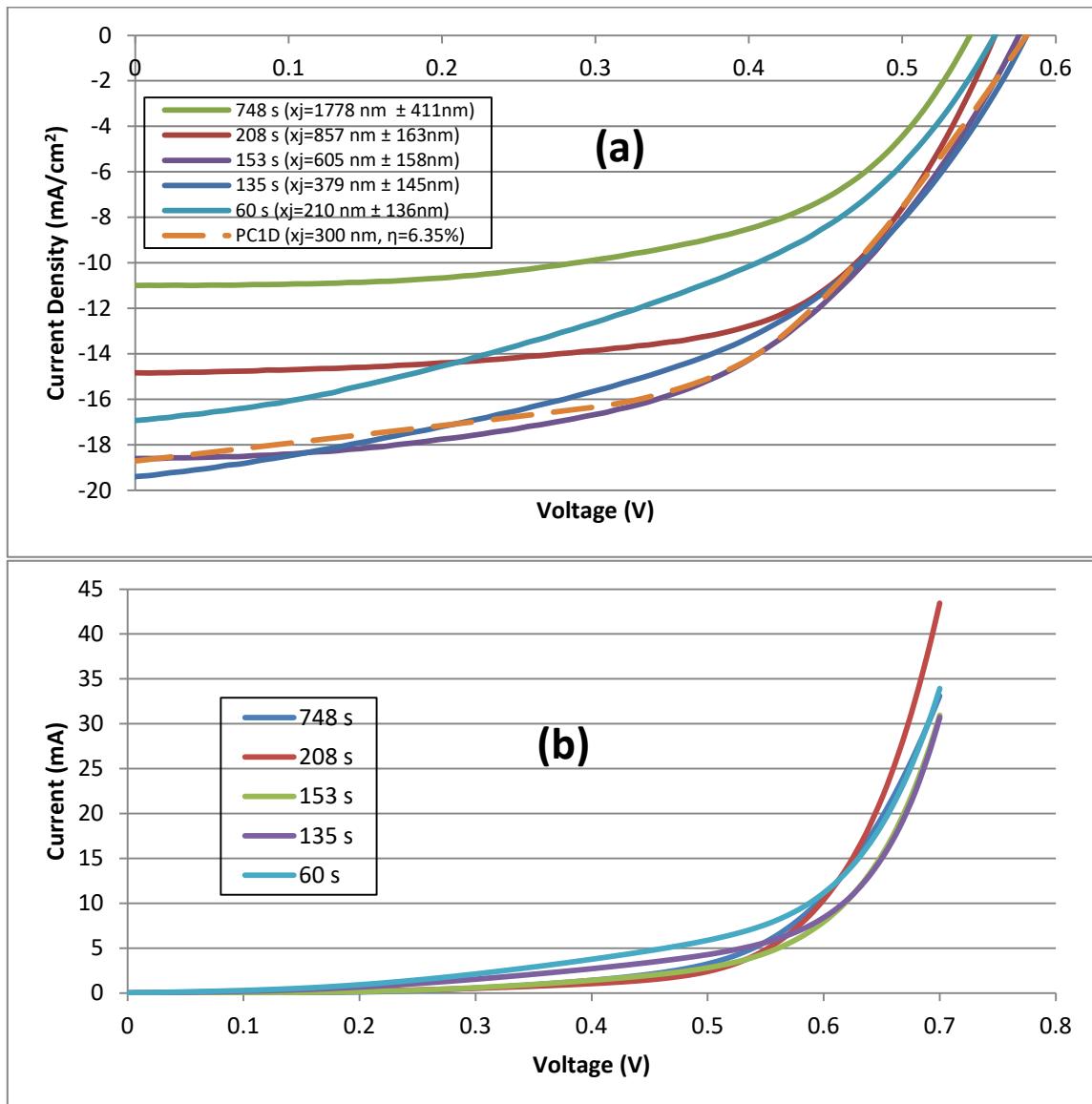


Fig 94 (a). Light and (b). Dark I-V curves for various diffusion times highlighting the effect of junction depth on device performance

As the three shortest runs undertaken all had a peak hold time of five seconds but with reducing ramp up and ramp down times it was decided that an alternative means of defining the diffusion time was necessary. The times shown, therefore, are the total that each diffusion process spent over 800 °C. This is broadly the temperature at which phosphorus

diffusion in silicon begins to occur at a meaningful rate and therefore provides a useful comparison between process runs (Fig 94).

Diffusion Time (s)	Junction Depth (nm)	Error (\pm nm)
748	1778	411
208	857	163
153	605	158
135	379	145
60	210	136

Table 8. Junction depth results for shallow emitter fabrication

It can be observed from Table 9 that a reduction in the junction depth from 1778 nm to 857 nm results in a 56% improvement in the current per area (J_{sc}) from 9.33 mA/cm² to 14.98 mA/cm² and a rise in absolute efficiency from 3.53% to 5.19%, a 65% relative improvement. When the junction depth falls to 605 nm, further improvements result with J_{sc} and efficiency rising to 19.32 mA/cm² and 6.01% respectively but with a reduction in fill factor. Reducing the junction further to 379 nm sees an increase in J_{sc} to 19.85 mA/cm² but a further fall in fill factor resulting in a fall in absolute efficiency to 5.38%. A final run was carried out to thin the junction even further, this time to \approx 210 nm, which saw J_{sc} fall to 17.22 mA/cm² and efficiency drop to 4.13%.

Diffusion Time	748 s	208 s	153 s	135 s	60 s
Junction Depth (nm)	1778 \pm 411	857 \pm 163	605 \pm 158	379 \pm 145	210 \pm 136
Voc (V)	0.54	0.56	0.57	0.58	0.56
J_{sc} (mA/cm ²)	9.33	14.98	19.32	19.85	17.22
Fill Factor (%)	56.90	61.98	54.50	46.81	43.02
R_{sh} (Ω cm ²)	1490	1135	975	178	222
R_s (Ω cm ²)	9.61	7.71	8.42	9.55	9.95
Efficiency (%)	3.53	5.19	6.01	5.38	4.13

Table 9. Performance parameters for devices with emitter thickness varied by diffusion time. Of note is the rising current density (J_{sc}) with reducing emitter thickness but associated fall in shunt resistance (R_s).

Plotting the real world device efficiency against the PC1D predicted efficiency in Fig 93 yields an interesting result. Whilst the maximum real world efficiency (\approx 6%) is similar to that predicted by PC1D, it occurs at approximately twice the thickness, i.e. 605 nm rather than the predicted 300 nm. Additionally, the real world efficiency then drops off significantly for further emitter thickness reductions compared to the predicted continued rise. This is likely due to the steadily increasing emitter resistivity resulting in poorer carrier collection and

greater resistance between the n-type emitter and the front surface contacts resulting in increased series resistance.

The dark I-V data is broadly consistent with the data in Table 9. In particular the effect of falling shunt resistance with reducing junction thickness is visible in the dark I-V curves with increasing current leakage. Additionally, the shape of the 208 second diffusion dark I-V curve is predictive of the best demonstrated fill factor under illumination.

Whilst the 153 second diffusion resulted in the best overall performance, it was too deep to be of use for application to the 1 μm pillar devices. The 135 second diffusion's junction depth of 379 nm would leave 242 nm of p-type silicon core at the centre of the pillar. Taking into account the approximated depletion region width for this junction of ≈ 30 nm, the remaining electronically active p-type core is estimated to be ≈ 182 nm. Whilst a narrow margin, the loss of performance with shallower junction depths was quite severe and a reference device of $> 5\%$ was deemed desirable to ensure adequate resolution for assessing performance change versus pillar devices. It was decided, therefore, to proceed with the 379 nm thick emitter for pillar device fabrication.

6.8. Conclusions

- The development of Proximity Rapid Thermal Diffusion (PRTD) as a process for fabricating silicon solar cells has been described.
- The PRTD process is capable of rapidly diffusing highly doped but shallow emitters using no toxic gases or specialised diffusion equipment and with total thermal processing times of less than three minutes. Whilst not a new process, there is little evidence in the literature of PRTD being used for the fabrication of solar devices. Hence this work has generated new knowledge in this area.
- Diffusion by PRTD is significantly improved by the addition of oxygen to the nitrogen carrier gas. The sheet resistance falls from over $300 \Omega/\square$ to $\approx 25 \Omega/\square$ and the uniformity of the diffusion improves by a factor of ten with the addition of 2.5% oxygen to the nitrogen carrier. The addition of oxygen may also be responsible for the attainment of doping concentrations approaching the electronic limit of phosphorus in silicon (3×10^{20} atoms/cm 3) at temperatures lower than conventional theory would suggest is possible.
- Thick emitters ($> 1.5 \mu\text{m}$) prepared by the PRTD process demonstrated excellent shunt resistances ($\approx 1500 \Omega \text{ cm}^2$) but yielded poor values for J_{sc} of 9.33 mA/cm^2 , believed to be due to high front surface recombination due to the heavily doped emitter. Reduction of the emitter thickness to ≈ 605 nm supported this conclusion, as

J_{sc} rose to 19.32 mA/cm², with only a negligible ($\approx 2.5\%$) fall in fill factor for a total efficiency of 6.01%. Further reduction in emitter thickness to ≈ 379 nm yielded similar values for J_{sc} but a slight fall in absolute efficiency (5.38%) due to a falling fill factor. Additional reductions in emitter thickness led to further J_{sc} (17.22 mA/cm²) and efficiency losses (4.13%), indicating that further process refinement would be necessary to obtain significantly thinner emitters with useful performance.

- The efficiencies demonstrated by PRTD diffused planar cells are approaching the 6% predicted by PC1D for emitters with parameters similar to those possessed by the real world devices. This lends confidence to the use of modelling to inform future process development.

Chapter 7. Fabrication and Characterisation of Micro-rod Cells by Diffusion Doping

This chapter will discuss the fabrication of micro-rod solar cells using the proximity rapid thermal diffusion process detailed in Chapter 6. Subsequently, the performance of the devices will be described and analysed.

7.1. Pillar Device Fabrication

After development of a suitable diffusion recipe for application to pillar devices, the fabrication of these devices was undertaken.

Samples were first cleaned in an ultrasonicated acetone bath for five minutes followed by rinsing in running de-ionised water and then nitrogen blow dried. After this initial clean step the samples were subjected to a 20 minute piranha etch. Samples were then transferred to a de-ionised water rinse for 10 minutes before further rinsing in flowing de-ionised water and a nitrogen blow dry.

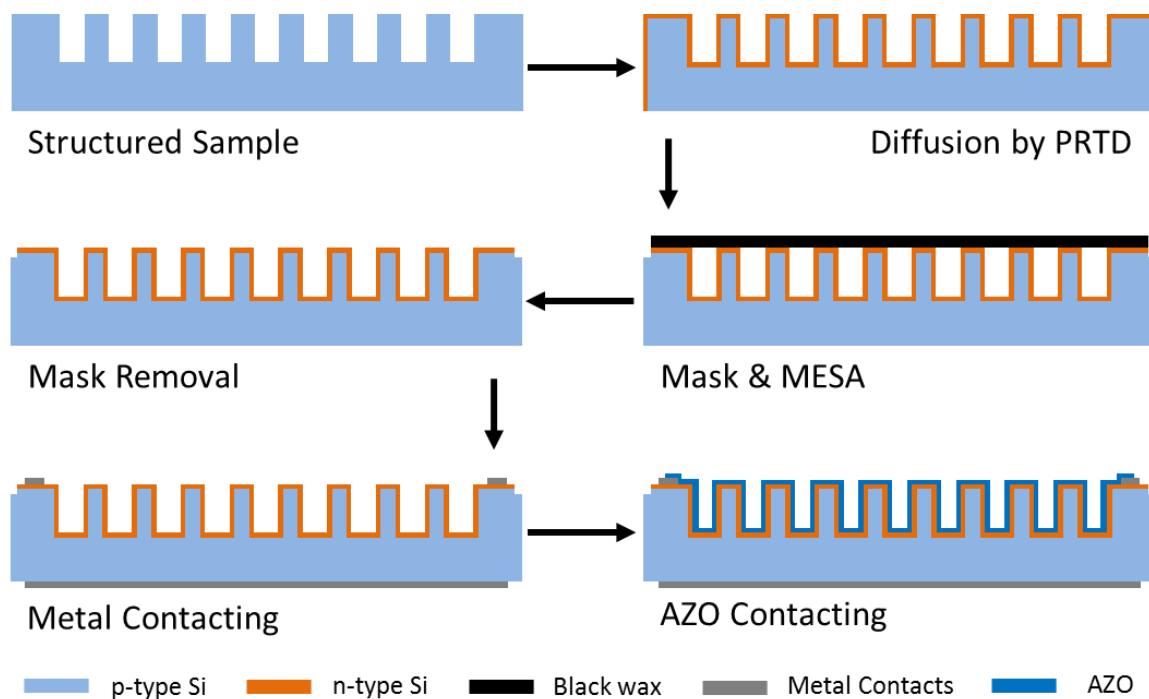


Fig 95. Pillar device fabrication process

At this point the samples were prepared to the necessary standard for diffusion and were loaded to the RTP system for the PRTD process. The diffusion was carried out at 1030 °C for 5 seconds using a 50% SOD concentration source wafer in a flowing 10% O₂ in N₂ process environment. The total RTP thermal cycle time, i.e. time above 800 °C, was 135 s.

This recipe was estimated to yield a diffusion depth of 379 ± 145 nm as described in Chapter 6 and deemed to produce the best compromise between junction depth and electronic performance from the planar emitter development.

The edge isolation and contacting steps are the same as those described for planar device fabrication in section 6.2 and are illustrated for pillar devices in Fig 95. After undertaking these post diffusion processes the devices were ready for I-V testing.

7.2. Pillar Device Performance Characterisation

Devices to be characterised were mounted on a thermal stage to maintain the required temperature of 25 °C, whilst a vacuum chuck ensured good contact with the rear side metallisation. The samples were shadow masked so that only the active pillar area was illuminated and a sprung contact probe contacted the front metallisation and consequently the transparent conductive oxide layer. The top contact and TCO arrangement are shown in Fig 96 for illustrative purposes (and described in section 6.7) and the device cross section is given in the last schematic of Fig 95. Additionally Fig 96 includes device dimensions showing the active device area to be 81 mm² and the total device to be 169 mm².

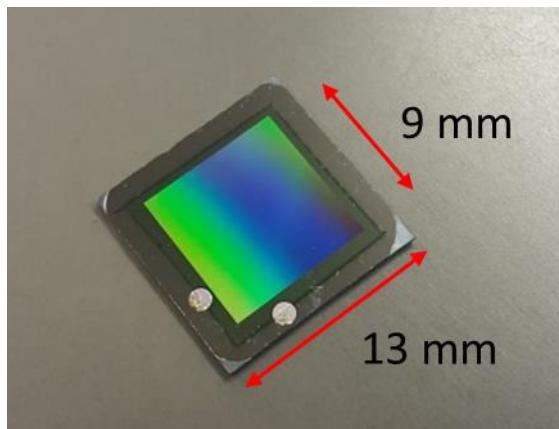


Fig 96. Plan view of pillar device showing Ni/Ag metal dots and AZO TCO layer. Dimensions shown are those of the active (9 x 9 mm) and total device areas (13 x 13 mm)

Dark I-V measurements were taken prior to illuminating the devices to ensure a good contact had been made and to investigate the performance of the device as a diode. The result of this sweep provided a crude indication as to the quality of the diffused emitter and of the applied contacting. The devices were subsequently illuminated by an AM1.5(G) spectrum with an applied voltage swept in the range of 0-0.7 V and the resulting current measured.

For clarity, the 1 µm and 10 µm diameter pillars are discussed in separate sections.

7.2.1. 1 μm Diameter Pillar Device Series I-V Analysis

The I-V curves shown below are those for the 1 μm diameter pillar devices with 1:1 (Fig 97a) and 2:1 (Fig 97b) pillar length to diameter aspect ratios. Also shown are the extracted device parameters for the devices shown in Table 10.

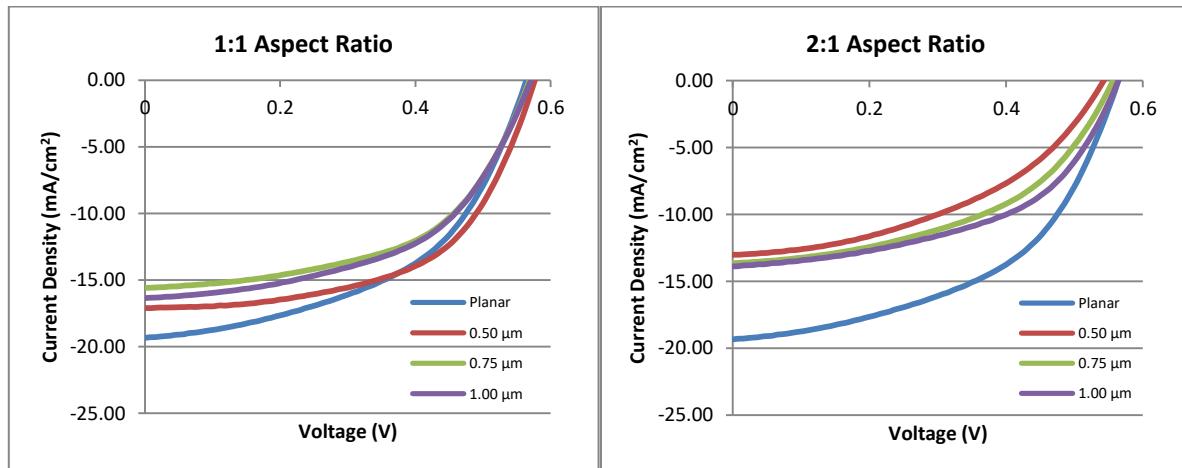


Fig 97. I-V data for 1 μm diameter pillar devices with: (a) 1:1 aspect ratio (b) 2:1 aspect ratio
(Legend describes inter-pillar spacing)

	1 μm Diameter - 1:1 Aspect Ratio					1 μm Diameter - 2:1 Aspect Ratio			
Pillar Spacing	Planar	0.50 μm	0.75 μm	1.00 μm	Pillar Spacing	Planar	0.50 μm	0.75 μm	1.00 μm
Voc (V)	0.553	0.574	0.568	0.572	Voc (V)	0.553	0.536	0.557	0.556
Jsc (mA/cm²)	20.05	17.76	16.18	16.97	Jsc (mA/cm²)	20.05	13.66	13.99	14.35
Fill Factor (%)	50.87	55.21	54.83	53.34	Fill Factor (%)	50.87	45.68	48.25	50.59
Rsh (Ω cm²)	554	760	812	583	Rsh (Ω cm²)	554	572	523	322
Rs (Ω cm²)	5.26	6.24	6.39	6.22	Rs (Ω cm²)	5.26	8.98	7.94	7.64
Efficiency (%)	5.64	5.63	5.04	5.18	Efficiency (%)	5.64	3.35	3.76	4.04

Table 10. Electronic performance data for 1 μm diameter pillar devices

The first feature of interest is the V_{oc} data as this was expected to be affected by the large surface area that is a feature of structured devices. There is no clear trend of V_{oc} being affected by surface area variation resulting from changing inter-pillar spacing alone. As the variation in total surface area between the extremes of pillar spacing (0.5 μm and 1 μm) for the 1:1 aspect ratio devices is only 35%, and when coupled with potential variation in the diffused emitter, this is not considered to be implausible. However, the variation in surface area between smallest and largest pillar spacing at 2:1 and 1:1 aspect ratios, respectively, is over 110% and therefore more likely to exhibit variation. To this end, the V_{oc} values of the planar, 1 μm 1:1 aspect ratio and 1 μm 2:1 aspect ratio devices where scatter plotted (Fig 98) against pillar length (with planar plotted as length zero). Additionally, the average

V_{oc} of the pillar lengths was plotted to highlight the generalised effect of varying surface area.

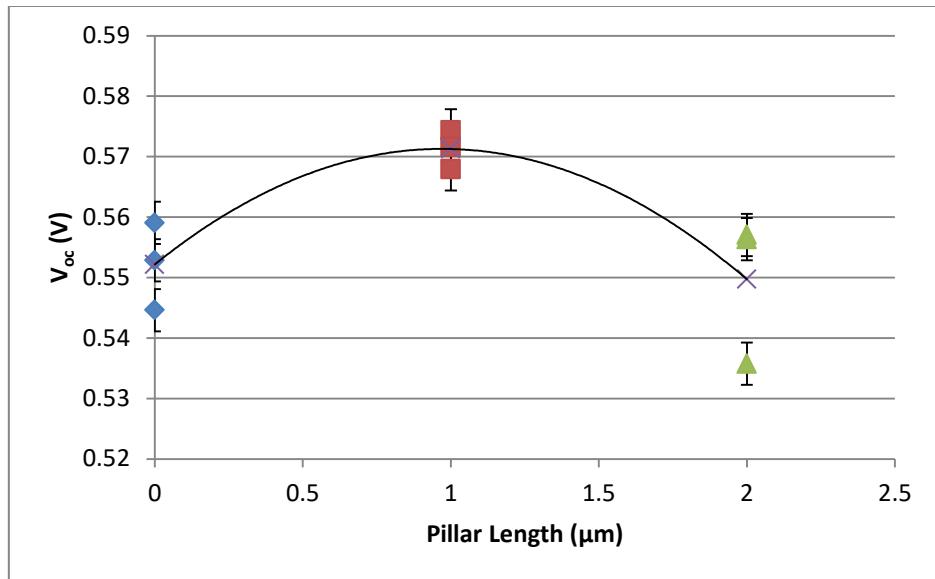


Fig 98. Effect of pillar length on 1 μm device V_{oc}

The structured devices exhibited an average V_{oc} improvement of 10-20 mV for pillar length of 1 μm compared to the planar control. The 2 μm pillars then exhibit an average fall in V_{oc} to a value slightly lower than that of the control. This is contrary to the results found by [124][280][302] which all suggested an average fall in V_{oc} between 10-50 mV for any non-planar geometry. In these cases the structures utilised were on the nano-scale, however, average losses of 20-40 mV for V_{oc} in structured devices compared to planar was also found by [303], this time for micron scale features.

Due to the small margins involved it is unreasonable to draw any significant conclusions from this data. However, one might cautiously state that this particular micron scale, low aspect ratio structure design appears to have at least a non-detrimental effect on device V_{oc} which is contrary to generally observed results.

The 1 μm 1:1 aspect ratio pillar devices all (with the borderline exception of the 0.50 μm sample) demonstrated inferior efficiency to the planar device, despite them demonstrating superior V_{oc} values and fill factors. Examination of their J_{sc} values suggested poor photocurrent generation which did not logically agree with the calculated absorption data for the devices. A similar situation was observed for the 1 μm 2:1 aspect ratio pillar devices with an even greater loss of J_{sc} exhibited in this case.

Plotting the J_{sc} data for the devices in a similar fashion to the V_{oc} data highlights the progressively decreasing average current density for increasing pillar length (Fig 99).

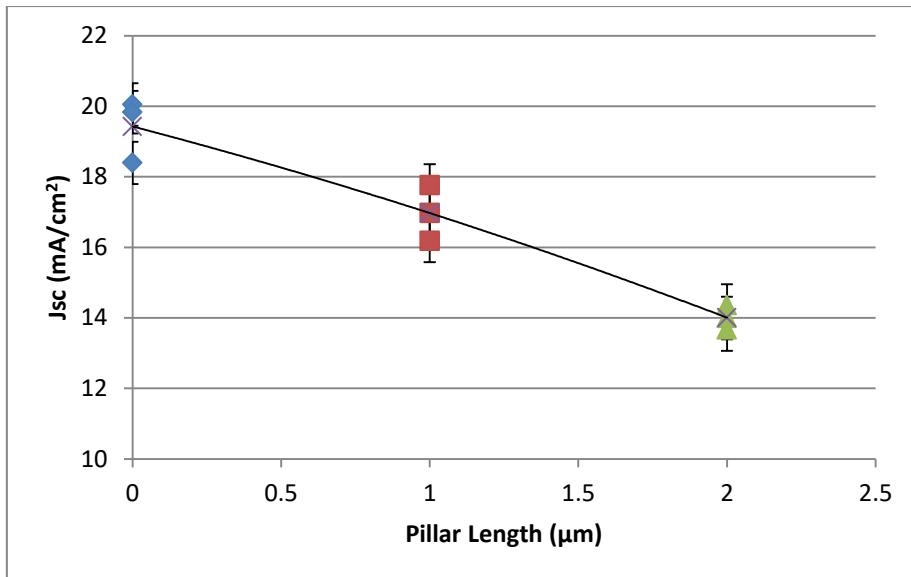


Fig 99. Effect of pillar length on 1 μm diameter pillar device J_{sc}

The general trend observed from the 1 μm diameter pillar J_{sc} data is contrary to what would be expected if a simple, greater absorption equals greater current, relationship is assumed. As the pillar devices are known to exhibit superior absorption to the planar device the problem was likely to lay with a generation issue.

The dark I-V measurements of the pillar devices were similar to that of the planar devices and under illumination the pillar devices still exhibited some current generation. This suggested that the basic device fabrication was not to blame, i.e. the junction and the contacts were fundamentally working. The assumption therefore was that a proportion of the incident light was being effectively absorbed by the device but not generating current.

The cause of the lost generation potential becomes apparent when the quantum efficiency data (Fig 100(a) & Fig 100(b)) from the devices is examined. It is apparent that incident light, particularly at short wavelengths, is less efficiently generating current in the pillar devices than in the planar devices and, more specifically, the loss of generation is generally more severe with increasing pillar density. The conclusion is, therefore, that the pillars themselves are taking a reduced role in generation and are instead primarily absorbing the shorter wavelengths (which are absorbed near to the front surface of the device).

A possible cause of this is variation in the diffusion process which could result in two potential outcomes. One is an excessively deeply diffused emitter, whilst the other is a non-uniform emitter which is deep at the top and shallow at the bottom of the pillars.

The former would lead to increased carrier collection losses in the n-type region. This would result because the short minority carrier lifetime in silicon with doping densities in the

$> 1 \times 10^{20}$ atoms/cm³ range means minority carrier diffusion lengths could be as low as 200 nm [136]. Therefore, carriers generated near to the surface would be unlikely to reach the edge of the junction to be collected. This is one of the key reasons why maintaining a thin emitter is crucial when high doping density is required. Additionally, if the increased emitter depth has also resulted in pillars with overlapping depletion regions in the p-type core, the whole structure will be likely to experience increased recombination with further consequences for device performance. This would explain why the J_{sc} loss becomes more severe with greater pillar length as an increasing proportion of the incident light is absorbed in these electronically compromised regions.

The latter possibility would result in areas of increased resistance at the pillar bases where the emitter is shallow. This would lead to current losses resulting from an inhibited flow of carriers generated in the upper portions of the pillars.

The likelihood is that a combination of both of the aforementioned cases is occurring, however, it is difficult to quantify either mechanism without the use of additional techniques which are discussed in further work in chapter 7.

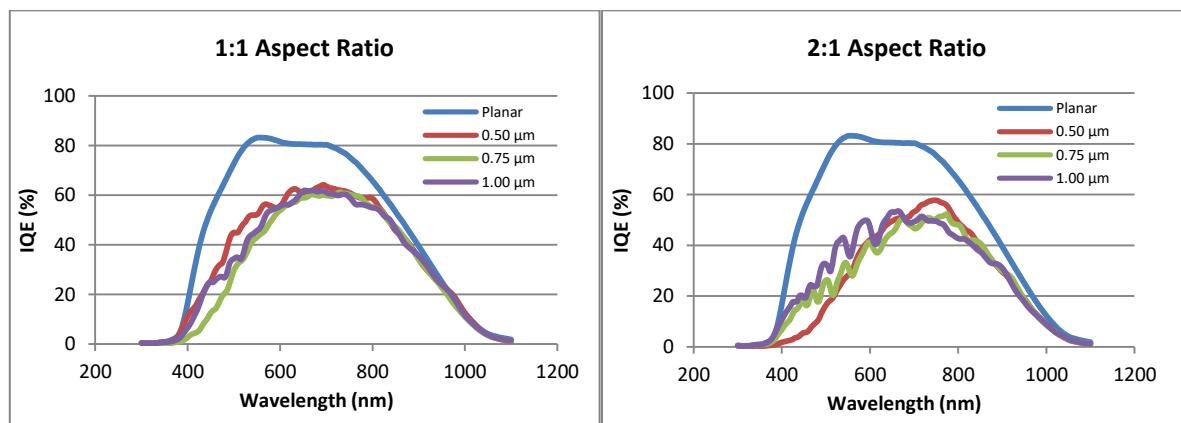


Fig 100. IQE data for 1 μm diameter (a) 1:1 and (b) 2:1 aspect ratio pillars with a planar device included for comparison (Legend describes inter-pillar spacing)

Whilst the reduced generation in the shorter wavelengths can be explained by previously discussed points, the reason for the lower generation in the longer wavelengths is not immediately obvious. A possible explanation is that, if the pillars are acting as regions of increased recombination, there are essentially inactive or dead gaps in the emitter where the electronically compromised p-type pillar cores meets the electronically active bulk p-type region (Fig 101). As a result, carriers generated below pillars would be required to travel further to reach the junction with an increased risk of recombination at the pillar base.

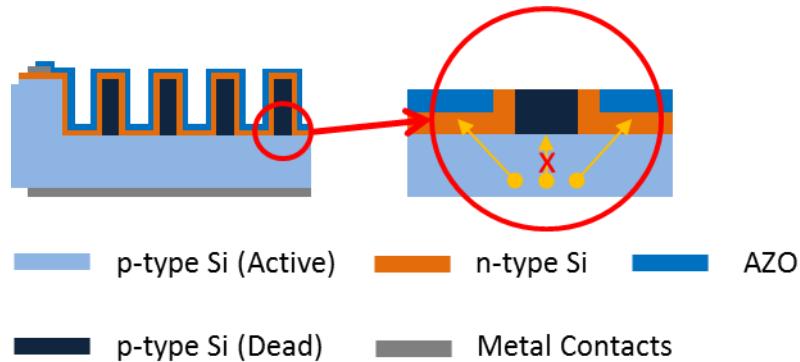


Fig 101. Effect of electronically inactive pillar cores on device performance

A final point worth of note is the values for shunt and series resistance. The shunt resistance values are somewhat low when compared to that of a refined cell, which would generally be greater than $1000 \Omega \text{ cm}^2$ [304]. This is likely due to the relatively thin and non-optimally passivated emitter. However, as will be discussed later in this chapter, this value is an improvement over that observed prior to the application of the AZO layer and not unreasonable given the device and emitter geometry. In a similar vein, the series resistance values are much higher than those which might be observed in an optimised device, which would typically be in the $\text{m}\Omega \text{ cm}^2$ range [305]. The effect of this high resistance is easily observable from the values for fill factor in Table 10 and the I-V curves in Fig 97. An ideal I-V curve would turn sharply upward at the maximum power point and continue near vertically to the V_{oc} value. Large series resistance has the effect of reducing the slope gradient, as is observed, and in turn reducing the fill factor. Once again, however, this value is an improvement compared to devices prior to application of AZO.

7.2.2. 1 μm Diameter Pillar Device Series I-V Analysis – Reduced Junction Depth

In an attempt to fabricate a non-depleted set of 1 μm pillar devices, modifications were made to the diffusion cycle carried out on the samples. The total cycle time was reduced to 60 s as this yielded a junction depth of $210 \pm 136 \text{ nm}$ in the earlier junction development work which, even allowing for error, should be adequately shallow not to deplete a 1 μm pillar.

Due to the previously found difficulties in effectively doping the 1 μm devices and, in particular the 2:1 aspect ratio structures, it was decided to apply the shorter process only to the 1:1 aspect ratio samples. Aside from the modified diffusion time, all other processing was carried out using the same steps as undertaken for previous device fabrication.

When the post diffusion checks of emitter sheet resistance were carried out, an anomalous value of $103.81 \pm 21.97 \Omega/\square$ was found. This was substantially higher than any previous value for diffusions undertaken in this time and temperature range. Despite this unexpected result, it was decided to proceed and devices were fabricated to assess their performance.

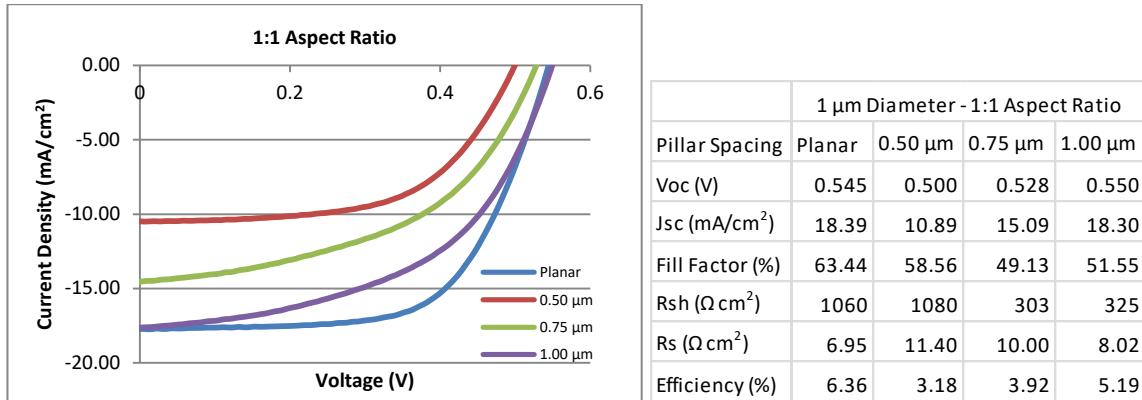


Fig 102 & Table 11. I-V data and parameters for 1 μm diameter pillar reduced thickness emitter devices (Legend describes inter-pillar spacing)

The first item of note is the improving V_{oc} values with increasing pillar spacing and therefore reducing surface area (see Table 11 and Fig 102). This result is in line with what would conventionally be expected for devices with a large surface area and suggested that a nominally conformal emitter may have been achieved. Conversely, however, a similar effect on efficiency and current generation was observed to the previous device series whereby devices with larger inter-pillar spacing performed better despite lower absorption. This supported the theory that the diffusion process itself was a factor in device performance.

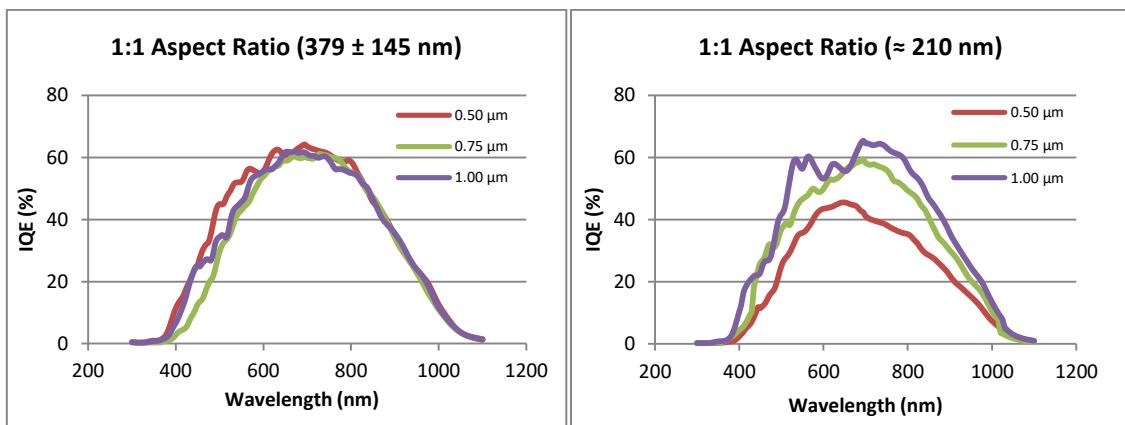


Fig 103. IQE data for (a) Original 1 μm pillar diameter series (b) Reduced emitter thickness 1 μm pillar diameter series (Legend describes inter-pillar spacing). Estimated emitter thickness is indicated in brackets after the aspect ratio.

Looking at the quantum efficiency data for the devices (Fig 103(b)) side by side with their previous series counterparts (Fig 103(a)) from the original diffusion process, it is evident that both the 0.50 μm and 0.75 μm devices are performing poorly. This was expected based on the parameters from the I-V data and can likely be attributed to their high series resistance which itself is probably a result of increased front contact resistance due to interfacing with a less highly doped emitter. Of note, however, is the 1 μm inter-pillar spacing device which, despite the high series resistance, achieves a J_{sc} value higher than both its counterpart and the highest performing device from the previous series. The reason for this can be attributed to the improved device IQE with both a higher peak value and better performance in the shorter wavelengths. This also suggests that, at least in the case of devices with shallower emitters, carrier generation and collection is taking place within the pillars themselves.

The reason for the higher sheet resistance and presumed resultant lower doping concentration in the devices is not immediately apparent but a possible explanation is as follows. As is discussed earlier in this chapter, the spin on dopant in this project utilises P_2O_5 , which in addition to being a phosphorus source, is also strongly hydroscopic. With repeated exposure to atmosphere, which occurs each time the container is opened to extract the SOD, some of the P_2O_5 absorbs water and becomes dilute phosphoric acid (H_3PO_4). Over time, as the volume of SOD is reduced and more of the remaining P_2O_5 is lost, the solution begins to lose its doping efficacy. It is believed, therefore, that in this case adequate P_2O_5 was available to dope the device n-type, but insufficient to achieve the peak doping concentrations previously obtained.

7.2.3. 10 μm Diameter Pillar Device Series I-V Analysis

The I-V curves shown below are those for the 10 μm diameter pillar devices with 1:1 (Fig 104a) and 2:1 (Fig 104b) aspect ratios.

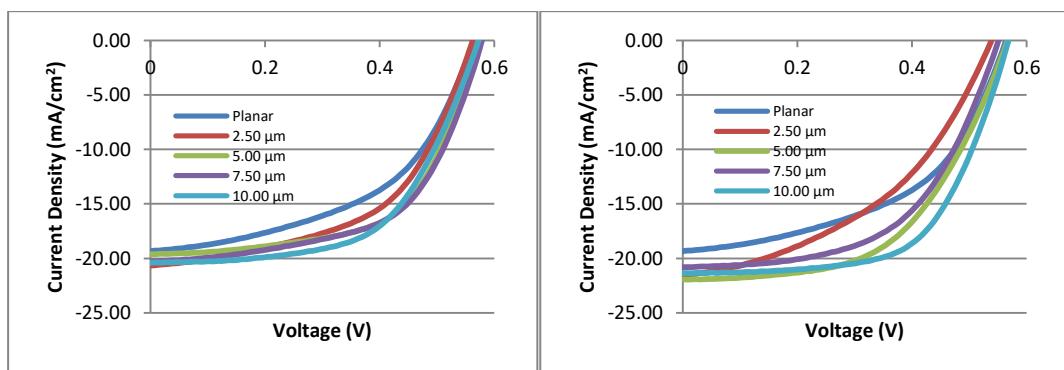


Fig 104. I-V data for 10 μm diameter pillar devices with: (a) 1:1 aspect ratio (b) 2:1 aspect ratio (Legend describes inter-pillar spacing)

The samples were diffused using the same PRTD conditions as the 1 μm pillar diameter devices (section 7.2.1.) with an emitter thickness of 379 ± 145 nm. The performance data for the devices shown in Fig 104 (a&b) are tabulated in Table 12. With regard to the V_{oc} values, as with the 1 μm diameter pillars, there is no clearly discernible trend for changes in surface area resulting from variable inter-pillar spacing at either aspect ratio. However, plotting the data in a similar fashion to that for the 1 μm pillars yields interesting results (Fig 105).

10 μm Diameter - 1:1 Aspect Ratio						10 μm Diameter - 2:1 Aspect Ratio					
Pillar Spacing	Planar	2.50 μm	5.00 μm	7.50 μm	10.00 μm	Pillar Spacing	Planar	2.50 μm	5.00 μm	7.50 μm	10.00 μm
V_{oc} (V)	0.553	0.565	0.575	0.578	0.574	V_{oc} (V)	0.553	0.539	0.568	0.551	0.571
J_{sc} (mA/cm^2)	20.05	21.38	20.39	21.13	21.16	J_{sc} (mA/cm^2)	20.05	22.22	22.87	21.63	22.19
Fill Factor (%)	50.87	51.91	60.58	58.16	59.63	Fill Factor (%)	50.87	42.53	53.87	55.45	60.64
R_{sh} (Ωcm^2)	554	243	769	668	958	R_{sh} (Ωcm^2)	554	193	544	666	669
R_{s} (Ωcm^2)	5.26	7.39	4.56	4.59	5.45	R_{s} (Ωcm^2)	5.26	8.03	6.08	5.72	5.16
Efficiency (%)	5.64	6.27	7.10	7.11	7.25	Efficiency (%)	5.64	5.10	7.00	6.61	7.68

Table 12. Electronic performance data for 10 μm diameter pillar devices

In a familiar pattern, the 1:1 aspect ratio pillars exhibit a slightly higher average V_{oc} to the planar devices before falling back to a similar value for the 2:1 aspect ratio devices. Notably in this case, two out of the four 2:1 devices exhibit V_{oc} values similar to the average for the 1:1 devices. This suggests that whilst the increased surface area may be a factor, the fabrication process might also be partly responsible and, if so, the average may be improved by refining this process. These results add to the earlier assertion that small aspect ratio micron-scale devices appear to be less detrimental to V_{oc} , as compared to nano-scale structures.

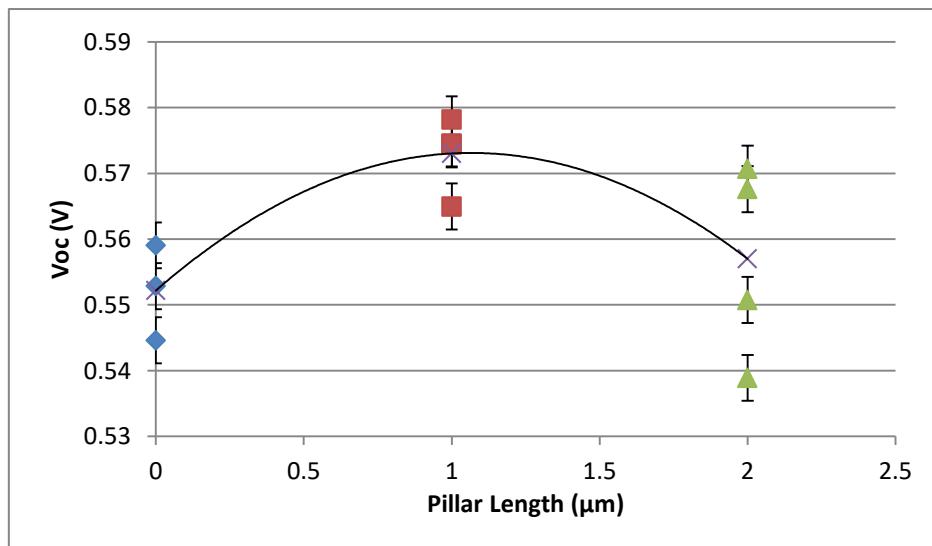


Fig 105. Effect of pillar length 10 μm on device V_{oc}

Considering overall performance, in contrast to the smaller 1 μm pillar devices, all but one configuration of the 10 μm diameter pillar devices demonstrates superior performance to the control devices with like for like processing. This lends further credence to the initial premise that larger micron scale structures, whilst demonstrating less effective anti-reflective properties, are favourable to overall electronic performance. The highest conversion efficiency achieved was 7.68% in the 2:1 aspect ratio device, showing an improvement of 36% over the planar reference cell efficiency of 5.64%. The lone structured device with inferior efficiency actually demonstrated superior J_{sc} to the planar device but for unknown reasons, assumed to be a processing problem, suffered a low fill factor and resultantly poor performance.

The most notable area in which the 10 μm devices demonstrate improved performance is their J_{sc} values. Plotting the average J_{sc} for each aspect ratio against pillar length (Fig 106) demonstrates the trend in generation predicted by theory for increased current generation with improved absorption. It is interesting that, if one compares the devices with the smallest and largest values for spacing, whilst their performance is reasonably similar the device with greater spacing and therefore poorest anti-reflection enhancement is in fact superior. There is a similar effect observable for the 2:1 aspect ratio 1 μm pillar devices whereby the most efficient device is that with the poorest absorption.

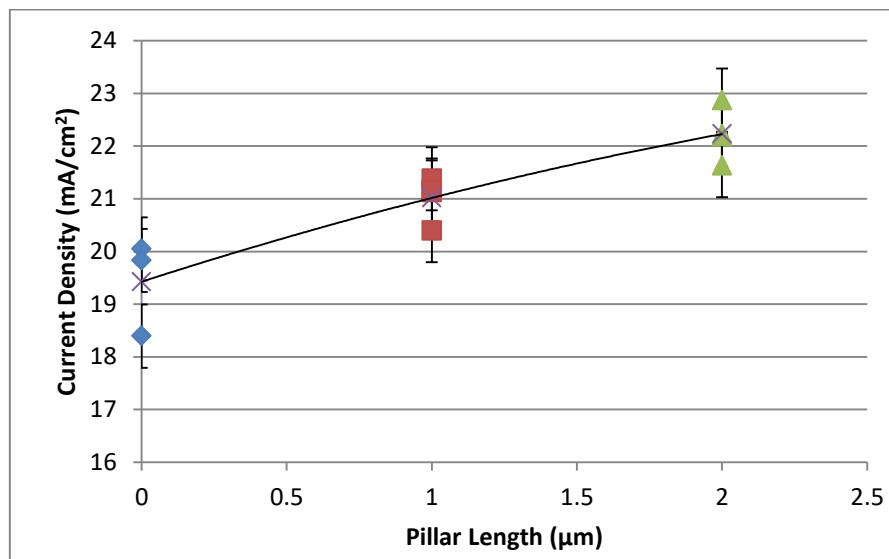


Fig 106. Effect of pillar length on all 10 μm diameter pillar device J_{sc} values

It may be suggested from this that the pillar spacing is affecting the emitter formation process, whereby the larger spacing results in a superior quality emitter and as a result better performance despite the poorer optical properties. There is some evidence for this when considering device fill factor, particularly for the 2:1 aspect ratio devices where the

potential for poor emitter uniformity over the length of the pillars is greater. It can be observed that with increasing pillar spacing there is a steady rise in device fill factor and also a decline in series resistance, suggesting a higher quality, more uniform emitter.

Fig 107 compares the best performing planar and 2:1 aspect ratio devices (10 µm spacing) with the device that possess the second best optical absorption (5 µm spacing). The second best device was selected over the best absorbing device (2.5 µm spacing) as the best optical device suffered significant electronic performance losses and did not provide a useful comparison.

The advantage of comparing QE rather than I-V data is that the current generated by the QE system's probe beam is very low and the effect of resistance is greater at higher currents [306]. It can be shown, therefore, that the 5 µm spacing device would be expected to perform even better than the 10 µm spacing device if other performance limiting factors were reduced. This is broadly as would be expected for a purely, absorbance equals current relationship, where losses are neglected.

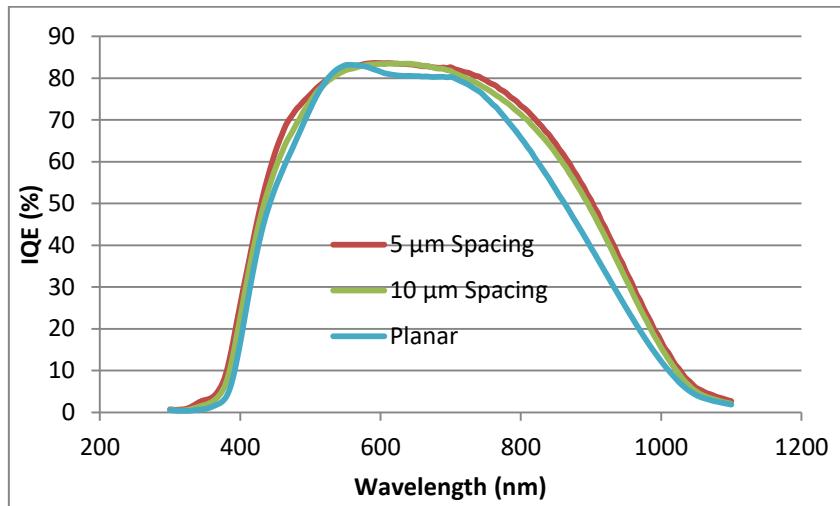


Fig 107. IQE data demonstrating superior theoretical performance of 5 µm spacing device to best performing 10 µm spacing device

It is in fact possible to approximate the J_{sc} that might be expected from the two considered devices if electronic performance losses were minimised. This is achieved by taking the responsivity data of the devices as measured to calculate their QE, multiplying the response at each wavelength interval x (in $A \cdot W^{-1}$) by the equivalent irradiance value from the measured AM1.5(G) spectra y (in $W \cdot m^{-2}$) and summing the resulting current values. The result must then be corrected from the calculated area of 1 m^2 to the area of the device

under investigation, in this case 0.81 cm^2 and converted to millamps from amps. This calculation is shown in Equation 6.8.

$$J_{sc} = \left(\sum_{300nm}^{1100nm} x A.W^{-1} \cdot y W.m^{-2} \right) \cdot 0.00081 \cdot 1000 \quad (6.8)$$

The resulting values for the devices in Fig 105 are given in Table 13.

Inter-Pillar Spacing	Short Circuit Current Density (J_{sc})
Planar	27.23 mA/cm ²
5 μm Spacing	36.08 mA/cm ²
10 μm Spacing	34.02 mA/cm ²

Table 13. Calculated J_{sc} from device response data

Even if the figures are assumed to be aspirational rather than truly achievable, it is apparent that there is the potential for some quite significant improvements in the performance of the devices. The data also infers that a device with smaller inter-pillar spacing, and therefore better absorption, should exhibit superior current generation as expected by theory.

7.2.4. The Effect of a Deeper Junction Applied to 10 μm Pillars

It was evident from characterisation data that the major performance limitation to the devices under investigation is the relatively poor fill factor with the major contributor to this believed to be the series resistance. In an attempt to eliminate the emitter as a potential source of series resistance, a longer diffusion process was undertaken to produce a much thicker emitter which should possess low resistivity and good charge separation. Ensuring good charge separation was important as this is another potential source of poor fill factor [140] and needed to be eliminated to confirm that the major device performance limiting factor was series resistance.

The devices were fabricated by the same method as those discussed in the previous section with the only modification being a diffusion time of 768 seconds rather than the previous 135 seconds. As a result, the measured junction depth increased from $379 \pm 145 \text{ nm}$ to $1778 \pm 411 \text{ nm}$. The measured sheet resistance fell from $15.36 \pm 1.6 \Omega/\square$ to $7.34 \pm 0.5 \Omega/\square$ indicating a deeper, more heavily doped emitter. The I-V curves and parameter data are shown below in Fig 108 and Table 14.

It should be noted that the poor planar performance is as a result of the deposited AZO front contact overlapping the edge of the device and producing a shunt path between the two

sides of the junction. Additionally, the missing 2.5 μm inter-pillar spacing device is as a result of sample breakage during processing.

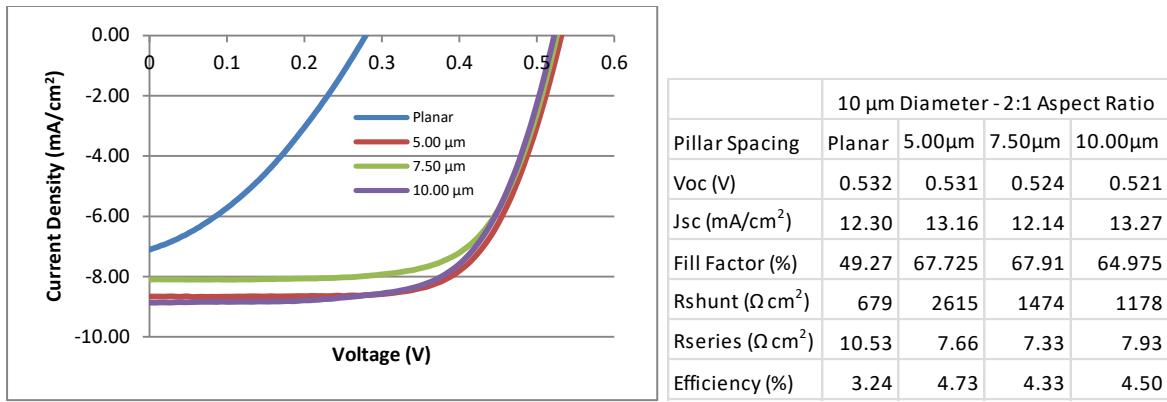


Fig 108 & Table 14. I-V data and parameters for deep diffused emitter (Legend describes inter-pillar spacing)

The most obvious change that has occurred is the fall in J_{sc} which is in agreement with the experimentation earlier in this chapter. Deep emitters cause very high recombination rates in the front of the device and as a result the current generation suffers accordingly. The other obvious feature is the consistently high shunt resistances that are attained. Whilst the emitter is still unlikely to be of uniform thickness, it is now adequately thick that there should be few regions shallow enough to cause significant shunting.

From the I-V data it is clear that the thicker junction has somewhat improved the fill factor of the devices compared to those fabricated with the thinner emitter, rising from an average of 56.65% to 66.87%. This suggests that the shallow emitter is not optimised and part of the poor fill factor is indeed due to incomplete charge separation at the junction. However, looking at the approximated series resistance values, it is clear that increasing the junction depth and reducing its sheet resistance has had a negligible effect on the series resistance. In this case it has in fact risen slightly from $6.25 \Omega \text{ cm}^2$ to $7.64 \Omega \text{ cm}^2$.

This result suggests that a major source of the series resistance observed across all the fabricated devices tested is as a result of the contacting schemes utilised. If one considers the thickness of the applied metallisation layers to the devices which are on the order of 1 μm and compares this to 20 – 30 μm of contact thickness as applied to commercial devices this is perhaps unsurprising. However, as the series resistance values across all the devices tested are relatively consistent, this lends confidence to the validity of inter-device and inter-series comparison.

7.2.5. The Effect of AZO Films on Device Shunt Resistance

It has already been demonstrated in chapter 5 that AZO possesses useful anti-reflection properties which are beneficial to device performance from an optical absorption point of view. However, its primary purpose is as a TCO layer acting as a wide area front contact.

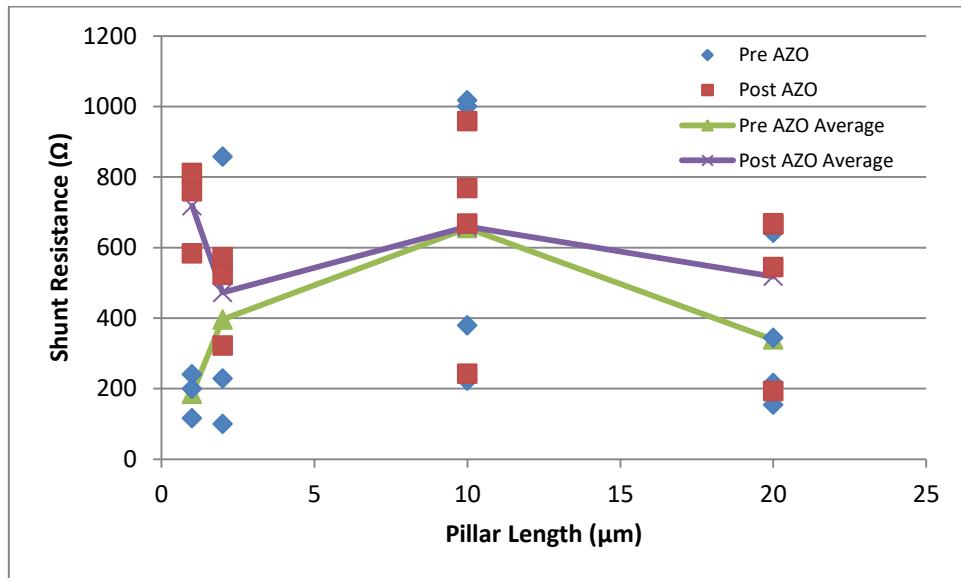


Fig 109. Plotted shunt resistances of all pillar devices with 379 ± 145 nm deep emitter and average for devices at each pillar length. Note that in this case, pillar length is described rather than aspect ratio (i.e. 1 μm and 10 μm pillars are 1:1 and 2 μm and 20 μm are 2:1)

It was predicted that the TCO layer would reduce the series resistance of the devices, compared to those with edge only metal contacts, and indeed this was observed. What was not initially expected, however, was the effect the AZO would have on shunt resistance.

Fig 109 is a plot of all of the calculated shunt resistance values for devices plotted against their length both before and after the application of the AZO TCO layer. Also plotted is the average shunt resistance value for each pillar length before and after the AZO TCO was applied.

It can be observed that there is a substantial average improvement of nearly 250% for the 1 μm diameter 1:1 aspect ratio devices. There is also a much smaller improvement of about 20% for the 1 μm diameter 2:1 aspect ratio devices.

The pre and post-AZO averages for the 10 μm diameter 1:1 aspect ratio devices are broadly similar which might be explained by the fact that these devices have a much smaller surface area and are therefore likely to be less prone to shunting. However, it should be noted that the pre-AZO average is high for this pillar length because of two exceptionally high values of

shunt resistance, whilst the other two values are more in line with the general pre-AZO values for shunt resistance. This is not to suggest that values are not accurate but rather that emitters formed by this process which naturally possess good shunt resistance are more commonly the exception than the rule. Therefore, under other circumstances, one might expect a greater difference. Finally, there is a little over 50% improvement in shunt resistance for the 10 µm 2:1 aspect ratio (2 µm pillar length) devices.

Clearly the application of AZO has a generally beneficial effect on the shunt resistance of the devices; whilst the exact reason for this enhancement is not immediately apparent; a possible explanation is discussed here.

It is well understood that any area of a solar device where the junction is exposed causes large recombination currents in the depletion region [307], commonly referred to as J_{02} (I_{02} in chapter 2 of this work) in the ideal diode equation. Due to the significant potential for the junction in the structured devices to be exposed by either damage to the pillars or non-uniform diffusion it is likely the devices will exhibit increased J_{02} current. These regions of localised high recombination appear effectively as shunts in the junction [308] and will reduce the overall device shunt resistance if not effectively passivated.

To examine the effect of AZO on passivating this kind of shunt requires a means of extracting the J_{02} value. This is commonly achieved by fitting the double diode equation to the dark I-V data of the devices; however, this is process intensive and requires good approximations of the initial device parameters. An alternative analytical method is proposed in a paper by Chan and Phang [309] which requires only the illuminated I-V parameters; V_{oc} , I_{sc} , V_{max} , I_{max} , the thermal voltage V_T and initial approximations for series (R_{S0}) and shunt (R_{Sh0}) resistances extracted from the I-V curve slope at V_{oc} and I_{sc} respectively.

Their method involves reducing the double diode model down into a series of equations that produce dimensionless parameters (α , β , γ and δ) shown in equations 6.9-6.12.

$$\alpha = I_{sc} - \frac{V_{oc}}{R_{Sh0}} \quad (6.9)$$

$$\beta = I_{sc} - I_m - \frac{V_m}{R_{Sh0}} \quad (6.10)$$

$$\gamma = \exp\left(\frac{V_m - V_{oc}}{2V_T}\right) \quad (6.11)$$

$$\delta = \frac{I_m}{V_T} \quad (6.12)$$

These values are then combined using equations 6.13-6.15 to find dimensionless variables a, b and c:

$$a = \alpha\gamma\delta(1 - \gamma) \quad (6.13)$$

$$b = \alpha\gamma(2 - \gamma) + \alpha\gamma\delta R_{s0}(\gamma - 1) - \beta + \gamma\delta V_T(1 - 2\gamma) \quad (6.14)$$

$$c = \alpha\gamma R_{s0}(\gamma - 2) + \beta R_{s0} + 2\gamma V_T(1 - \gamma) \quad (6.15)$$

which are input into a quadratic equation (equation 6.16).

$$aR_s^2 + bR_s + c = 0 \quad (6.16)$$

This equation can then be solved by the standard solution for quadratic equations (equation 6.17) to obtain a value for R_s .

$$R_s = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \quad (6.17)$$

From this point a series of equations (equations 6.18-6.21), derived from the double diode model and with the required parameters isolated, can be solved using the obtained value for R_s and the aforementioned I-V parameters.

The solutions for I_{s1} (J_{01}), I_{s2} (J_{02}), R_{sh} and the photo generated current (I_{ph}) are then:

$$I_{s1} = \left(\frac{V_{oc}}{R_{sh0}} - I_{sc} + \frac{2V_T}{R_{s0} - R_s} \right) \exp - \left(\frac{V_{oc}}{V_T} \right) \quad (6.18)$$

$$I_{s2} = \left(I_{sc} - \frac{V_{oc}}{R_{sh0}} + \frac{V_T}{R_{s0} - R_s} \right) \exp - \left(\frac{V_{oc}}{2V_T} \right) \quad (6.19)$$

$$R_{sh} = \left(\frac{1}{R_{s0} - R_s} - \frac{I_{s1}}{V_T} \exp \frac{I_{sc} R_s}{V_T} - \frac{I_{s2}}{2V_T} \exp \frac{I_{sc} R_s}{2V_T} \right)^{-1} \quad (6.20)$$

$$I_{ph} = I_{s1} \left(\exp \frac{V_{oc}}{V_T} - 1 \right) + I_{s2} \left(\exp \frac{V_{oc}}{2V_T} - 1 \right) + \frac{V_{oc}}{R_{sh}} \quad (6.21)$$

A modification was required and made to this model as it assumed a solar cell with values for diode ideality factors close to the optimum, i.e. $n_1 = 1$ and $n_2 = 2$. This was clearly not the case for the devices under examination with n_2 expected to be particularly high as a result of the series resistance, similar to that seen in [303][310][311][121]. These values appear in the diode equations in front of the V_T parameter, which is the thermal voltage of the device and is typically 0.02586 V at 25 °C. To permit modification of the n_1 and n_2 parameters, the n_1 variable was inserted in front of the lone V_T values and n_2 replaced the value of 2 in front of

the $2V_T$ variable in all equations where they occur. For example, the I_{ph} equation (6.21) becomes (changes highlighted in bold):

$$I_{ph} = I_{s1} \left(\exp \frac{V_{oc}}{\mathbf{n}_1 V_T} - 1 \right) + I_{s2} \left(\exp \frac{V_{oc}}{\mathbf{n}_2 V_T} - 1 \right) + \frac{V_{oc}}{R_{sh}} \quad (6.22)$$

By applying the discussed technique to data for known devices and adjusting the diode ideality factors to achieve a matching modelled and measured value for I_{ph} it was then possible to extract approximations for I_{s1} (J_{01}), I_{s2} (J_{02}) and R_{sh} . The calculated values for R_{sh} matched well to those predicted by the slope at J_{sc} adding confidence to the values produced for I_{s1} (J_{01}) and I_{s2} (J_{02}).

	Modelled J_{02} Pre-AZO	Modelled J_{02} Post-AZO	Change (%)
Planar	1.84E-07	1.15E-08	93.78
10 μm 1:1 Aspect Ratio			
2.5 μm	5.10E-09	8.66E-08	-1598.87
5 μm	2.23E-08	2.14E-08	3.98
7.5 μm	9.51E-08	4.89E-08	48.62
10 μm	1.10E-07	3.02E-08	72.56
10 μm 2:1 Aspect Ratio			
2.5 μm	3.85E-07	3.89E-07	-0.89
5 μm	2.54E-07	1.04E-07	58.98
7.5 μm	1.72E-07	1.05E-07	39.08
10 μm	1.56E-07	3.82E-08	75.45

Table 15. Effect of pillar length on device saturation current

Table 15 shows the calculated J_{02} for a planar device and the 10 μm 1:1 and 2:1 aspect ratio pillar devices. It is generally the case that J_{02} current is reduced post application of the AZO layer which may be indicative of localised defects being passivated by its application. A significant exception to this is the 2.5 μm spacing 1:1 aspect ratio device which suffers a major increase in J_{02} current post application of AZO which is an agreement with a fall in estimated shunt resistance for this device. This particular device was an outlier which exhibited shunt resistance in excess of 1000 Ω cm² as fabricated and the reasons for the reduction post application of AZO are unclear.

With the current analysis, it is not possible to say with certainty that passivation of localised high recombination shunt defects is a significant cause of device improvement. Furthermore, it is likely that some improvement results from passivation of the highly doped front surface which will suffer high recombination in general as discussed in chapter 2. The work required to quantify either of these factors in detail is beyond the scope of this project. However, it is

apparent that AZO has significant potential for use in solar devices beyond simply as a TCO, both as an AR coating (as seen in chapter 5) and potentially as a passivating layer.

7.3. Conclusions

- The fabrication of pillar devices using proximity rapid thermal diffusion and their characterisation has been described in this chapter.
- Achieving effective diffused emitters in 1 μm diameter pillars proved to be a challenging undertaking. For an estimated emitter depth of $\approx 380 \text{ nm}$, the efficiency of these devices was in general below that of reference planar cells ($\approx 5.6\%$) with J_{sc} falling with increasing pillar length. Quantum efficiency measurements suggested this was due to poor photocurrent generation. A possible cause of this is non-uniform doping of the pillars down their length with excessively deep junctions at the top and inadequate doping at the bottom. Interestingly there was no clear trend of V_{oc} being adversely affected by the surface micro-structuring or pillar density. This is in contrast to the behaviour of nanowire devices which generally show a loss in V_{oc} compared to reference planar devices.
- Reducing the diffusion time and, hence, emitter depth to a shallower $\approx 210 \text{ nm}$ for the 1 μm diameter devices led to improved current generation and performance in the lowest density devices with a pillar spacing of 1 μm indicating the beneficial effects of shallower emitters. Notably, the best J_{sc} rose from 17.76 mA/cm² for the previous $\approx 380 \text{ nm}$ thick emitter to 18.30 mA/cm² despite a $\approx 2 \Omega \text{ cm}^2$ increase in series resistance. It is likely that with further refinement of the diffusion process, more effective devices could be produced.
- The larger 10 μm diameter pillars demonstrated better and more consistent results, adding weight to the argument of offsetting less efficient anti-reflection properties of larger microstructures with superior electronic performance. Their J_{sc} values were found to increase with increasing pillar length in line with expectation. The highest conversion efficiency achieved was 7.68% in the 2:1 aspect ratio devices showing an improvement of 36% over the planar reference cell efficiency of 5.64%. Estimations of J_{sc} from IQE data ($\approx 34 \text{ mA/cm}^2$) suggest potential for significantly higher values compared to those observed ($\approx 22 \text{ mA/cm}^2$).
- Similarly to the 1 μm diameter devices the 10 μm diameter devices appear to be less detrimental to V_{oc} with the results indicating at least equivalent V_{oc} to planar devices. With the literature generally indicating a definite loss in V_{oc} in nano-scale structures it is an area which invites further investigation.

- Increasing the estimated emitter depth in the 10 μm diameter pillars from ≈ 379 nm to 1778 nm by increasing the diffusion time lead to an increase in FF from $\approx 57\%$ to $\approx 67\%$ and high shunt resistance values above $1000 \Omega \text{ cm}^2$. Unfortunately, the efficiencies were sub 5% due to the high series resistance and low J_{sc} values, a contributory factor for the latter likely being increased recombination losses due to the deeper emitters. Whilst the emitter was still unlikely to be of uniform thickness, it was probably adequately thick with fewer regions shallow enough to cause significant shunting.
- In addition to acting as an AR layer and a wide area top contact for the cells, the application of AZO on top of the emitter layers was found to have a generally beneficial effect on the shunt resistance of the devices. An analysis of the I-V characteristics indicated a reduction in the recombination saturation current density J_{02} after application of AZO. Hence, it is possible that the AZO acted as a passivating layer to reduce recombination. Further work is required to confirm this and also to reduce the relatively high series resistance from all the devices suffered, and which was determined largely to be due to the front contacts.

Chapter 8. Conclusions and Further Work

This chapter will summarise and conclude the findings of this project and discuss areas which could be developed upon.

8.1. Conclusions

- Pillar devices with structured areas of 81 mm^2 were fabricated by stepper optical lithography and deep reactive ion etching (DRIE) in collaboration with Phillips Innovation Services, Eindhoven. These are mature, commercial technologies and would permit wafer-scale area patterning of devices.
- Pillars with diameters of $1 \mu\text{m}$ and $10 \mu\text{m}$ and length:diameter aspect ratios of 1:1 and 2:1 were fabricated with varying inter-pillar spacing values. The $1 \mu\text{m}$ diameter pillars demonstrated, on average, a 40% reduction in reflection compared to planar silicon whilst the $10 \mu\text{m}$ pillars achieved a 10-20% reduction.
- The deposition of an electronically optimised transparent conductive oxide (TCO) in the form of aluminium doped zinc oxide (AZO) was achieved by sputter deposition. This was undertaken using a compound target and lower substrate temperature ($< 300^\circ\text{C}$) compared to that required for the more common ITO ($> 500^\circ\text{C}$).
- Whilst primarily a TCO, the AZO was found to possess useful anti-reflective properties. It was found to be possible to deposit conformal coatings of AZO to the pillar structures which resulted in a 50-60% reduction in reflection over planar silicon for the $10 \mu\text{m}$ diameter pillars and over 70% for the $1 \mu\text{m}$ features. This is in agreement with discussion in literature which proposed the use of multiple anti-reflection strategies for larger scale structures.
- There was also some initial evidence to suggest that AZO possessed some passivating properties, with values for saturation current generally found to fall post application of an AZO layer.
- The various configurations of the $1 \mu\text{m}$ diameter pillars were modelled optically in collaboration with City University London using the Lumerical FDTD modelling package. Comparison of the modelled and measured reflection demonstrated good correlation lending confidence to the use of modelling to inform the design of future structuring schemes. This was believed to be the first systematic study of identical geometry modelled and fabricated devices, particularly on the micron scale.
- Silicon micro-rod solar cells with emitters formed by proximity rapid thermal diffusion (PRTD) were fabricated with a peak efficiency of 7.68% compared to 5.64% for planar devices prepared by the same technique. It is believed that this is the first time

that this process has been used in conjunction with structured devices for PV purposes.

- Devices with 10 µm diameter pillars generally demonstrated superior performance to planar devices with the “champion” device achieving a 2% absolute improvement and the majority of other devices demonstrating at least a 1.4% improvement.
- The 1 µm diameter pillar devices generally exhibited performance equivalent to or slightly lower than their planar counterparts. This is believed to be due to emitter uniformity issues resulting from the developmental nature of the PRTD process used. Refinement of the process yielded encouraging results which suggested that with further refinement the 1 µm diameter pillars could also demonstrate effective efficiency enhancements.
- All devices with 1:1 aspect ratio demonstrated minor improvements (10-20 mV) to V_{oc} , whilst the 2:1 aspect ratio devices exhibited V_{oc} values broadly similar to the planar control. This was generally contradictory to the literature which almost invariably exhibited a loss of 10-50 mV in V_{oc} for any device with increased surface area compared to planar. Due to the small sample size it would be unreasonable at this stage to state categorically that small aspect ratio features have a non-detrimental or even beneficial effect on device V_{oc} , however, it is clearly an area worthy of further consideration.
- Despite the rod length clearly affecting the V_{oc} there is no obvious trend between pillar spacing and V_{oc} or J_{sc} as might have been expected. It is conceivable that with a larger sample set trends might emerge, however, it is more likely that emitter variation cause by the non-optimised diffusion process is overwhelming any tendency for the data to conform to a pattern. It was noted in the results for the 2:1 aspect ratio devices at both pillar diameters that generally higher efficiencies and superior fill factors are found for larger inter-pillar spacing. This suggested that the doping process was affected by the pillar geometry and as has been mentioned previously requires refinement to prevent it being a cause of performance variations.
- The PRTD process permitted the diffusion of n-type emitters with a diffusion time of less than three minutes and a total process cycle time of less than ten minutes. This was achieved without the use of toxic process gases or diffusion specific hardware. Good uniformity was achieved with further improvements believed possible by adjustments to the carrier gas flow rates.
- The growth of emitter layers on structured devices by chemical vapour deposition (CVD) was demonstrated with good conformity. The electronic properties of the films

were non-optimal but this was deemed to be due to equipment limitations and with refinement could provide an alternative means of emitter formation.

- An area which was challenging for all devices was series resistance which was determined to be due to the front contacts requiring further optimisation. The necessity of a TCO to provide a conformal contact to the structured devices added complexity to the contacting scheme and requires further investigation.

8.2. Further Work

The most significant area which has shown itself in need of development through this project is the proximity rapid thermal diffusion emitter formation process. Whilst clearly not ineffective, the process was believed to be suffering from uniformity issues when applied to structured devices. Whilst demonstrating good uniformity on the sheet resistance mapped planar devices it was considered likely that dopant was not being effectively deposited into the regions between structures. This theory was supported by the observed poorer performance for longer pillars and those with narrower spacing. This was believed to be a cause of the indistinct performance variation with varying pillar spacing as well as a contributory factor to the low fill factors observed. The main cause of this variation is believed to be linked to the high flow rate of the process gases used during diffusion resulting in a turbulent diffusion atmosphere. The high flow rate was necessitated due to limitations in the operable range of the rapid thermal processing (RTP) systems mass flow controller (MFC). Due to its minimum operating flow rate of 40 sccm and a need to mix the gas down to 2.5% O₂ in N₂, an N₂ flow rate of at least 1600 sccm was required. It is proposed that the reduction of the operating range of the O₂ MFC such that the optimised 10% O₂ in N₂ diffusion atmosphere could be achieved for a lower N₂ flow rate would result in better inter-feature deposition and diffusion of the dopant.

An alternative approach would be to utilise a diffusion furnace with a POCl₃ phosphorus dopant source. Subject to appropriate control and uniformity of gas flow, it is possible that this process would permit uniform deposition and drive in of dopant to the structured devices. However, a limitation of the diffusion furnace approach is the potential for variation in final emitter depth due to the lack of fine control over diffusion cycle time and temperature. A variation of this process would see the doped oxide layer grown on the surface at a low temperature ($\approx 800^{\circ}\text{C}$) followed by transferring the samples to an RTP system for the drive in process. This is effectively equivalent to directly applying an SOD solution to the surface of the devices, however, because the doped oxide is deposited from the gas phase it reduces the application difficulties because of the non-planar surface.

Clearly of major benefit to any of the aforementioned approaches would be a means by which the emitter could be accurately monitored. The ball grooving and staining approach used in this project demonstrated good results but was limited to testing emitter depth on a planar control device which provided no guarantee of equivalent results on the pillar devices. The use of a technique such as secondary ion mass spectrometry (SIMS) [312] would permit the analysis of emitter depth at localised points on structures and allow analysis of the uniformity of the diffusion process. From an electronic point of view, the application of the electron beam induced current (EBIC) technique [313] would permit the analysis of the current generation process within the devices. From this it would be possible to establish the electronic effectiveness of the diffused emitter and identify overly thick areas with high recombination or thin areas which inhibit current flow.

Another area which would benefit from further refinement is the contacting processes utilised within this work. The rear contact, whilst not significantly more resistive than commercial or laboratory devices would still likely be improved by switching from the existing sputter deposition to screen printed paste. This would immediately thicken the contact and permit optimisation of the firing process without the risk of incorporating excessive aluminium into the melt and leaving a thin and resistive or even non-existent contact pad.

Of more significance would be development of the front contacting scheme. Whilst it has been demonstrated that the AZO used in this work has resistivity that is comparable with best achievable, the means by which device current is extracted from the TCO itself has not been considered. In the current device geometry the AZO is simply deposited such that it lays atop the Ni/Ag dot contacts at the edge of the device. This requires that the full device current is extracted across the device area to a single contact point which will almost certainly lead to an increased series resistance. An optimised geometry would likely include depositing a metal frame around the planar edge of the front of the device atop the AZO such that the maximum distance that current must travel in the AZO is half the device diameter.

Furthermore, it has been noted that AZO in addition to being an effective TCO layer also demonstrates useful AR properties as well as possibly acting as a passivating layer. The AR properties are not in doubt but are subject to thickness optimisation which may run contrary to best electronic performance; however, it is likely that an effective compromise between the two is achievable with further development. The evidence for the passivating capability of AZO is less clear cut and whilst it clearly has some benefit on device performance, significant further work would be required to quantify this benefit and define the actual mechanism by which it is effective.

Regarding the pillar structures themselves, whilst the larger features have demonstrated good electronic properties, their optical properties would benefit from further refinement. It is likely that longer features would have a beneficial effect on light trapping, however, based on the existing fabrication process this would not be possible. An alternative approach is to modify the shape of the features to improve their anti-reflection properties, similar to that demonstrated in [314]. Clearly, however, any modifications must remain compatible with effective emitter fabrication and conformal front contact deposition to prevent compromised device performance.

The final area worthy of mention is the application of the pillar structures to thin silicon. The application of the masking, etching and contacting processes to thin multicrystalline silicon deposited from the gas phase should in principle be achievable using the techniques described here. However, emitter formation and effective device performance would likely be limited due to the variable material quality. The ideal application of the pillar structures is therefore to thin monocrystalline or polycrystalline silicon which should support effective electronic device fabrication. Thin monocrystalline silicon is typically difficult to achieve as wafer sawing is generally limited to thicknesses in excess of 100 µm. Whilst thinning by wet etching can achieve uniform wafers as thin as 2 µm [315], it is process intensive and a high material loss process. An alternative technique has been demonstrated [316] which describes the exfoliation of multiple, individual thin crystalline layers which could serve as substrates for structuring and device fabrication. Epitaxially thickened polycrystalline silicon is another possible approach to the problem and as it can be prepared on a low cost substrate such as glass or foil [317] it reduces potential handling difficulties which are inherent with thin substrates. Clearly suitable thin silicon, whilst challenging to fabricate, is becoming more readily available and a requirement for effective performance enhancing schemes to facilitate its efficient use in PV devices is likely to follow. This work has demonstrated that micron-scale; low aspect ratio rod structures may be suitable for this application and, subject to emitter refinement and contact optimisation, it should be possible to fabricate them with existing processes.

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Appendix A – Silicon Nitride as a Diffusion Barrier

Using a diffusion barrier to prevent dopant diffusion into unwanted areas requires a deposited layer through which diffusion either cannot occur or proceeds suitably slowly that the required impurity diffusion can be completed before dopant permeates the barrier layer. Silicon nitride (SiN) is a common choice as it is straightforward to deposit and demonstrates excellent resistance to diffusion for relatively thin barrier layers.

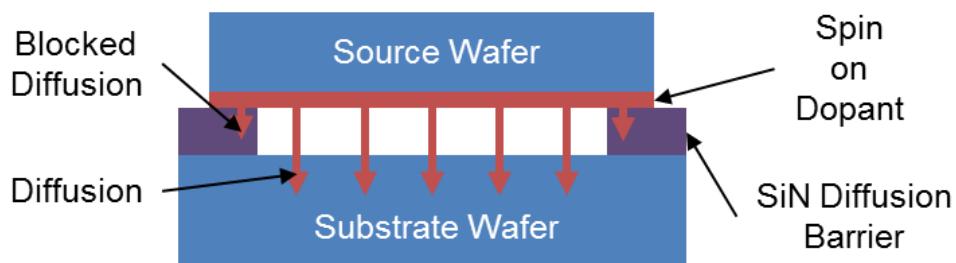


Fig I. The arrangement of source and substrate for proximity thermal diffusion (PTD). The diagram highlights the barrier effect of the silicon nitride (SiN), with the diffusion undertaken by placing the stack in a tube furnace. Note that the SiN is drawn significantly over thickness for illustrative purposes.

To assess its performance, a number of 15 mm^2 p-type $<100>$ $0.1\text{-}0.5 \Omega/\text{cm}^{-1}$ samples were prepared by acetone cleaning and piranha etch to act as samples to be doped. Prior to loading to the sputter system for SiN deposition the samples were dipped in a 2% hydrofluoric acid solution to remove the native surface oxide present on the silicon wafer. This ensures the best possible bonding of the SiN to the wafer surface rather than incorporating an intermediate interlayer. The area of the samples to be diffused was masked from SiN deposition using polyimide tape which was removed post deposition. The silicone based adhesive is designed to leave no surface residue but to ensure the highest level of surface purity the samples were subject to an additional piranha etch after the SiN deposition and prior to the diffusion process.

The samples were doped using a technique referred to as proximity thermal diffusion (PTD), which was originally trialled as a means to carry out all the doping in this project. All samples were diffused in a tube furnace at 900°C for 30 minutes in a flowing 1000 sccm atmosphere of nitrogen. The source was a p-type $<100>$ silicon wafer with a layer of 4% SOD applied by spin coating and cleaved into 14 mm^2 samples. These were placed atop each sample to be diffused and acted as individual localised dopant sources (see Fig I).

Post diffusion the samples were dipped in a 10% HF acid solution to remove the residual glassy oxide from the diffusion process. It was observed that this also removed the SiN

barrier layer which was notable as SiN generally demonstrates a reasonable resistance to HF. This is believed to be due to the sputter deposition process used and the non-optimised stoichiometry of the film.

The devices were then contacted with a wide area aluminium contact on the rear and bi-layer Ni/Ag 1.5 mm dot contacts on the front surface (as described in section 6.7). I-V testing was carried out under dark conditions and 1.5AM(G) illumination to assess the performance of the diffused emitter. Values for shunt resistance were estimated from the slope of the I-V curve at short circuit current (I_{sc}).

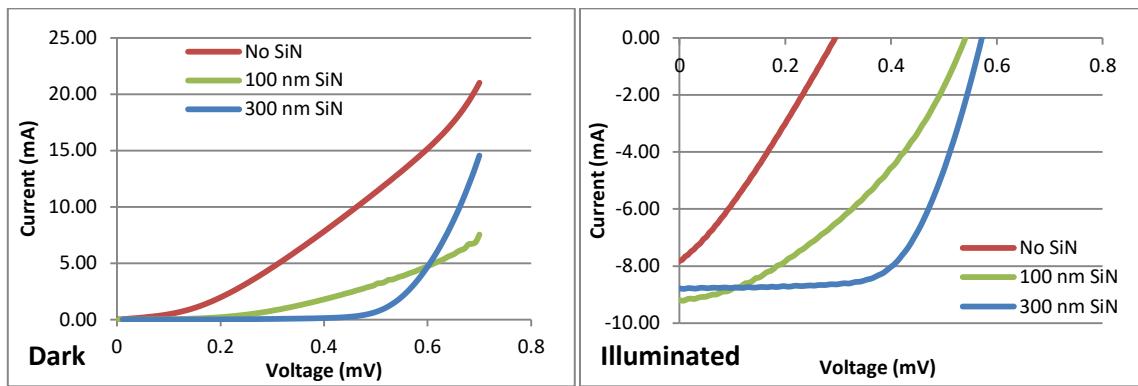


Fig II. Effect of diffusion barrier thickness on device I-V performance. Increasing the barrier thickness significantly raises V_{oc} as well as improving I_{sc} to a lesser extent

It is apparent from both the I-V curves (Fig II) and the parameter table (Table I) that devices with no form of diffusion barrier have substantially degraded performance. The shunting is sufficiently severe to affect the open circuit voltage which is generally fairly immune to all but the most poorly designed devices.

The devices diffused with a 100 nm SiN barrier show an immediate improvement with V_{oc} rising to > 540 mV which is more in keeping with that expected of a silicon device. The fill factor of the device is still poor, however, suggesting that the SiN has not been entirely effective at preventing diffusion in the masked area. Raising the thickness of the diffusion barrier to 300 nm has a significant effect, with fill factor rising to $> 60\%$ and a V_{oc} value approaching 570 mv. Overall device efficiency is still relatively low ($\approx 5\%$) but this is a feature of the large emitter depth and high doping concentration resulting in poor carrier generation.

Whilst this approach yielded reasonable device performance it had two key flaws. Firstly, it relied on a diffusion process which demonstrated poor emitter uniformity, likely resulting from uneven dopant transport due to a lack of carrier gas movement between the source and the sample to be doped. Secondly, it was incapable of preventing emitter wrap around from

dopant which might enter the diffusion atmosphere from the source and deposit on the sides or rear of the sample to be doped.

	No Diffusion Barrier	100 nm Diffusion Barrier	300 nm Diffusion Barrier
V_{oc} (V)	0.295	0.541	0.572
I_{sc} (A)	7.83×10^{-3}	9.20×10^{-3}	8.78×10^{-3}
Fill Factor (%)	29.22	39.41	64.17
Efficiency (%)	1.05	3.05	5.02
R_{Shunt} ($\Omega \text{ cm}^2$)	55.8	195	393

Table I. Diffusion Barrier Sample Parameters

In principle it would have been possible to develop the masking and sputter deposition process to apply the diffusion barrier to all surfaces of the device to be diffused, making the technique usable with the PRTD diffusion process ultimately utilised. However, this would have required multiple process steps with no guarantee that the diffusion barrier would be effective every time. Furthermore, the addition of multiple steps would remove the advantage of the process whose main attraction was simplicity of application. Hence, whilst effective for testing the diffusion barrier technique, this approach was ultimately ruled out for further work.

Appendix B – List of publications

Published

1. Oates, F. J. Cabrera-España, A. Agrawal, and H. S. Reehal, "Fabrication and characterisation of Si micropillar PV structures," in *Proceedings of Photovoltaic Science, Applications and Technology 10*, 2014.
2. Oates, F. J. Cabrera-España, A. Agrawal, and H. S. Reehal, "Fabrication and characterisation of Si micropillar PV structures," *Mater. Res. Innov.*, vol. 18, no. 7, pp. 500–504, Nov. 2014.
3. Oates, H. S. Reehal. "Proximity rapid thermal diffusion for emitter formation in silicon solar cells," in *Proceedings of Photovoltaic Science, Applications and Technology 12*, 2016, pp. 7-10.
4. F. J. Cabrera Espana, A. Agrawal, H. Reehal, and A. Oates, "Hut-Like Pillar Si Solar Cells," *Conference on Lasers and Electro-Optics*, OSA Technical Digest (2016) (Optical Society of America, 2016), paper SF2P.3.

In Preparation

1. Oates and H. S. Reehal, "Fabrication and characterisation of Si micro-pillar solar cells".
2. A Oates, A Agrawal, H S Reehal "Optical properties of Si micro-pillar structures coated with sputtered ZnO:Al thin films".
3. A. Oates, H. S. Reehal. "Development of proximity rapid thermal diffusion for n-type emitter formation in silicon solar cells".