Effect of diffusion parameters on emitter formation in silicon solar cells by proximity rapid thermal diffusion

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N-type emitters have been formed in p-type monocrystalline silicon with good uniformity and high peak doping concentration by proximity rapid thermal diffusion (PRTD). High diffusion rates are achievable for relatively low temperatures (< 1000 °C) with the addition of O2 to the N2 diffusion atmosphere. Solar cells have been prepared from the diffused samples to assess their performance and efficiencies of up to 6.0% have been achieved. The devices possess high series resistance and high recombination rates amongst other factors which limit their performance. Reducing the junction depth improves Jsc and efficiency but is accompanied by degrading shunt resistance and FF for junction thicknesses below ~400 nm. Further refinements of cell processing should improve efficiency and result in a diffusion process for forming shallow emitters for application to microstructured devices such as micropillar radial junction solar cells.

*Diffusion, rapid thermal processing, emitter formation, silicon solar cells*

1. Introduction

Silicon wafer solar cells dominate the solar PV market with ~90% market share [1]. The drive to reduce costs is targeting thinner Si wafers and more complex cell geometries including nano- and micro-wire designs with radial p-n junctions [2–4]. Formation of the p-n junction is a key stage in the cell fabrication process and is traditionally carried out in conventional thermal furnaces using solid or gaseous dopant sources. Ion implantation has also recently made inroads in PV manufacturing [5]. These techniques can have limitations in terms of control of junction depth and/or uniformity when applied to 3 dimensional structures such as micro and nanowire solar cells which require shallow junctions. Whilst ion implantation unquestionably permits fine concentration control and repeatability, it has a significant limitation when applied to 3D structured devices as complex tilt and rotation schemes are necessary to achieve uniform dopant distribution.

An alternative means of shallow junction fabrication is through the use of rapid thermal processing (RTP). Several RTP approaches including the use of spin on dopant (SOD) sources [6] or grown dopant oxides [7] deposited either directly on a sample to be doped [8], or on a sacrificial wafer acting as a solid dopant source [9], are reported in the literature. All have demonstrated the ability to form controllable, shallow junctions in silicon and indeed the directly applied SOD and grown oxide methods have been used to produce photovoltaic devices [10]. This approach, however, is potentially problematic for nano and microstructured devices due to the difficulty of applying conformal coatings of the dopant source to non-planar surfaces.

In this paper we concentrate on proximity rapid thermal diffusion (PRTD) as a means to fabricate shallow emitters with a view to doping micro-structured silicon solar cells [11]. This is a noncontact diffusion process that uses a sacrificial dopant source (referred hereafter to as a source wafer) prepared by spin coating a silicon wafer with a SOD. The source wafer is placed in proximity to samples to be doped. When heated, mass diffusion of the dopant from the SOD layer results. This is transported in the gas phase to the surface of the samples to be doped where adsorption and diffusion occurs [12]. By controlling the diffusion time and temperature it is possible to accurately control junction depths and dopant profiles [13].

There is little evidence in the literature of PRTD being used for the fabrication of solar devices. This paper presents results for PRTD diffused emitters in planar monocrystalline silicon solar cells. The aim is to develop the process to form radial junction micro-pillar solar cells.

1. **Experimental**

As supplied, p-type, 1-10 Ω cm, <111> orientated silicon wafers were used as dopant source carriers whilst 0.1‑0.5 Ωcm, <100> orientated wafers were used as the substrate for diffusion. Prior to use they were subjected to a piranha clean process (3:1 – H2SO4:H2O2) to remove organic contamination, followed by rinsing with de-ionised water and drying in a steam of nitrogen.

Dopant source wafers were prepared by coating them with SOD; a 4 wt% solution of phosphosilicate polymer in a solvent carrier (supplied by Filmtronics). Different SOD concentrations were studied by diluting the as supplied solution with methanol. The solution was applied by spin-coating at 1000 rpm for 30 seconds to produce a uniform film. The wafers were then baked at 200 °C for 30 minutes in air to drive off residual solvent.

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*Fig 1. Equipment configuration for proximity rapid thermal diffusion*

The samples to be diffused were prepared by cleaving the Si wafers into 13x13 mm2 pieces. These were placed atop a Si wafer acting as a mechanical carrier in the RTP system (Fig 1). The dopant source wafers were placed facing the samples using Si spacers to maintain a 0.5 mm gap between them. These were then loaded into the RTP system on top of a silicon carrier wafer. Silicon spacers were placed around the edge of the carrier before the source wafer was placed atop these to complete the diffusion stack. After loading, samples were subjected to diffusion processes with temperature varied in the range 770 °C – 1030 °C and a variety of cycle times.

The RTP system was an Annealsys AS-One 100 capable of supporting a 100 mm diameter wafer. It was pumped with a Varian SH-110 dry scroll pump. The diffusion was undertaken in an atmosphere of flowing electronic grade nitrogen (N2) and oxygen (O2). Typical thermal cycles for diffusions consisted of a fast ramp (<60s) to the peak diffusion temperature followed by a hold period which was varied in the range 1-15 mins. At the end of the hold period the temperature was ramped down to 500 °C over a short period (≈180 s).

To analyse the depth of the junction produced, ball grooving and staining was used on selected samples. This technique consisted of forming a groove in the doped silicon substrate using a steel ball coated with a diamond paste to expose the diffused region and underlying substrate. A staining solution consisting of hydrofluoric acid, chromium trioxide and de-ionised water was then applied which created a visible contrast difference between the two regions. By measuring the radii of the two differentiated regions, combined with the known radius of the steel ball, the junction depth was calculated [14].

Solar cell fabrication was carried out as shown in Fig 2. After diffusion and emitter formation, MESA edge isolation was performed by masking and wet etching the samples. Apiezon Wax W was used as the masking layer. Subsequently, a 1 μm thick layer of Al was sputtered onto the rear and annealed at 500 °C for 30 secs in the RTP system to form an ohmic back contact to the p-type substrate. Front side contacting to the n-type emitter was achieved by sequentially evaporating bi-layer nickel-silver (15nm and 1000nm thick respectively) dots of 1.5mm diameter around the edge of the front surface. The front contacts were annealed at 420 °C for 15 min in a tube furnace under nitrogen flow to form ohmic contacts. Finally, a transparent conducting oxide (TCO) layer of Al doped ZnO (AZO) was sputter deposited on the front surface to reduce front surface series resistance and complete the device structure. From the initial 13x13 mm2 silicon pieces, the final cell size was 9x9 mm2 after processing.

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*Fig 2. Device fabrication steps with emitter formed by proximity rapid thermal diffusion.*

The cells were tested at 25 °C under AM1.5(G) illumination using a class A solar simulator and a Keithley 2400 Sourcemeter to sweep and measure the current-voltage characteristics. Four point probe measurements were used to map the sheet resistance of the diffused wafers. Additionally, the oxide layer thickness formed on the surface during the diffusion process was measured by ellipsometry to investigate the effect of the various diffusion parameters on its formation.

1. Results and Discussion

The influence on diffusion of the SOD concentration, process gas flow rates and diffusion temperature was studied by measuring the oxide layer thickness formed during the diffusion process and the sheet resistance after the oxide had been stripped off in HF acid. Multiple 13x13 mm2 samples were loaded into the centre of the RTP chamber during each run. The standard deviation of the average surface sheet resistance for each of the samples from a diffusion run, indicated by error bars in the figures below, was used an indicator of diffusion uniformity.

* 1. **SOD concentration and N2 flow rate**

In PRTD, phosphorus from the SOD layer evaporates as phosphorus pentoxide (P2O5) and is transported to the silicon wafer substrate by gas phase diffusion. Adsorption and surface reaction processes lead to reduction of the dopant oxide and formation of a silicon oxide layer according to equation (1) [15].

|  |  |
| --- | --- |
|  | (1) |

The phosphorus is incorporated into the oxide forming a phosphosilicate glass. This glassy layer then becomes the dopant source with phosphorus diffusing from this layer into the silicon by interstitial dopant diffusion, the primary means of phosphorus transport in silicon [16].

The influence of SOD concentration on sheet resistance and the thickness of the oxide that forms on the Si surface during the diffusion process can be seen in Fig 3a. All diffusions were carried out at 870 °C for 15 minutes in a flowing 200 sccm nitrogen process atmosphere. Whilst 15 minutes is rapid compared to the time required by a diffusion furnace to achieve the same junction depth, it is difficult to define it as rapid in the true sense of PRTD. It was not apparent during the early stages of process development how significant the difference between conventional and rapid diffusion would be and as a result the relatively long diffusion time of 15 minutes was selected. SOD concentration is defined as percentage of the original concentration i.e. 100% is the as supplied 4% solution, 50% is 2% and so forth. Decreasing the SOD concentration leads to a decrease in the oxide thickness and an increase in the sheet resistance. Thisis accompanied by an increase in the sheet resistance standard deviation (shown by the error bars) indicating poorer uniformity. It is believed that this results from the low concentration of P2O5 in the N2 flow resulting in inconsistent adsorption onto the surface of the samples being doped.

This was further assessed by selecting a 50% concentration solution and repeating the previous diffusion parameters with differing N2 flow rates as shown in Fig 3b. Whilst the variation in sheet resistance between 200 sccm and 400 sccm is not significant, there is a tenfold increase in the standard deviation at 400 sccm as shown by the error bar. With increasing N2 flow the average sheet resistance increases, accompanied by a further increase in the standard deviation indicating poorer uniformity. This suggests that at the higher N2 flows an increasing proportion of the diffusing dopant may be being transported through the RTP system without being adsorbed at the substrate wafer surface. A decline in surface deposition and adsorption is further supported by the reduction in oxide thickness with increasing N2 flow.



*(a)*

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*(b)*

*Fig 3. Diffused emitter sheet resistance and grown oxide thickness with increasing (a) SOD concentration (b) N2 flow rate*

* 1. **Oxygen concentration**

The addition of O2 to the N2 carrier gas has a significant effect on both the average sheet resistance of diffused samples and the uniformity across the doped samples. This is shown in Fig 4 for a SOD concentration of 50%. All diffusions were undertaken at 870 °C for 15 minutes under 2000 sccm of N2 with O2 varied in the range 2.5% to 20%. It was necessary to utilise this high N2 flowrate in order to achieve low relative concentrations of O2 in the RTP system due to the delivery range and resolution of the O2 mass flow controller.



*Fig 4. Effect of oxygen on diffused emitter sheet resistance and grown oxide thickness*

The addition of excess O2 to the diffusion atmosphere increases the oxidation rate and modifies the diffusion mechanism occurring at the surface of the silicon. The oxide thickness increases approximately sevenfold under 2.5% O2 and continues to show a more gradual increase beyond this point. RTP has been shown to yield higher oxidation rates compared to conventional furnaces [17].

Under pure N2 sheet resistance values in excess of 300 Ω/□ were typical with standard deviation exceeding 30. The addition of 2.5 % O2 reduced both the sheet resistance and its standard deviation by an order of magnitude. It has been shown that phosphorus diffusivity is significantly enhanced in the presence of a growing oxide. This is believed to be due to the enhanced silicon self-interstitial formation under oxidation conditions and an associated increase in interstitial dopant diffusion [18]. Further increases in O2 up to 10 % had a negligible effect on the sheet resistance but did further improve the standard deviation (and diffusion uniformity) from 3.5 to 1.5. A high level of uniformity is particularly desirable when diffusing a conformal emitter into nano- or micro-wire devices.

Beyond 10% O2 the sheet resistance increases from an average of 25 Ω/□ to over 70 Ω/□ at 20% O2. This could be due to competitive surface reactions, with SiO2 growth occurring more rapidly than phosphorus can be incorporated into the phosphosilicate glass thus reducing the amount of dopant available to the silicon surface and leading to an increase in sheet resistance [19].

* 1. **Diffusion temperature**

The effect of diffusion temperature on sheet resistance and junction depth is plotted in Fig 5. All diffusions were undertaken for a period of 15 mins under 2000 sccm of N2 with 10% O2 addition. The data shows a significant decrease in sheet resistance between 770 °C and 870 °C. A smaller decrease occurs between 870 °C and 970 °C with virtually no change in the sheet resistance above 970 °C. The nominally exponential increase in junction depth with temperature is in agreement with the exponential relationship between diffusivity and temperature exhibited by phosphorus in silicon.

Approximations for peak doping concentration based on sheet resistance and the measured junction depth suggest an increase from 6 × 1019 atoms/cm3 at 770 °C rising to 1 × 1020 atoms/cm3 at 870 °C. A smaller increase from 1 × 1020 atoms/cm3 to 3 × 1020 atoms/cm3 between 870 °C and 970 °C is predicted as the electronically active limit of phosphorus in silicon (≈ 3 × 1020 atoms/cm3) is approached [20]. Above 970 °C there is little change in the sheet resistance despite a large increase in junction depth. Whilst the solid solubility of phosphorus in silicon increases above 970 °C (rising to a peak slightly greater than 1 × 1021 atoms/cm3 at 1100°C), none of the additional donors are electronically active above 3 × 1020 atoms/cm3 and able to increase conduction. An increase in temperature also serves to increase the diffusion rate of the phosphorus in silicon. This is in agreement with the results shown in Fig 5 with a significant increase in junction depth for a temperature increase from 970 °C to 1030 °C.



*Fig 5. Sheet resistance and junction depth vs diffusion temperature*

* 1. **Devices**

The emitter layers for devices were diffused at varying temperatures using a diffusion time of 15 min and a 50% SOD concentration source wafer. A 10% O2 in 2000 sccm of N2 process gas flow was employed.

The effect of increasing emitter depth (resulting from increased diffusion temperature) on device performance is illustrated by the current density (J)-voltage (V) data of Fig 6. Table 1 presents the device parameters extracted from this data. Fill factor can be observed to rise with increasing emitter thickness and doping concentration. Additionally, shunt resistance rises and series resistance falls with increasing junction depth due to the reduction in potential shunt paths and lower emitter sheet resistance, respectively. The thinnest emitter exhibits the highest series resistance, leading to the poor fill factor and shape of the J-V curve. Interestingly, the thickest emitter (1030 °C) has the lowest short circuit current density. This may be a result of the very high doping levels in the emitter layers (>1020 cm-3) leading to proportionally greater photocurrent losses for thicker emitters.

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*Fig 6. Light I-V curves highlighting the effect of varying junction depth (xj) caused by different diffusion temperature on device performance*

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| --- | --- | --- | --- |
| **Junction Depth (nm)** | **489** | **1051** | **1778** |
| Voc (V) | 0.56 | 0.57 | 0.54 |
| Jsc (mA/cm2) | 13.21 | 15.40 | 9.33 |
| Fill Factor (%) | 37.73 | 53.73 | 56.90 |
| Rsh (Ω cm2) | 117 | 370 | 1490 |
| Rs (Ω cm2) | 17.20 | 10.90 | 9.61 |
| Efficiency (%) | 3.43 | 4.89 | 3.53 |

*Table 1. Performance parameters for devices with emitter thickness varied by diffusion temperature*

Fig 7 and Table 2 show the effect of reducing the emitter thickness on performance. This was implemented by progressively reducing the diffusion time. A diffusion temperature of 1030 °C was selected as devices diffused at this temperature exhibited superior fill factors. Up to this point, diffusion time has been defined as the time spent at the peak temperature utilised. However, from this point it was re-defined as the total time each process spent above 800 °C. This is broadly the temperature at which phosphorus diffusion in silicon begins to occur at a meaningful rate and therefore provides a more useful comparison between process runs. This was necessary as the shortest diffusion runs had the same peak diffusion time but decreasing ramp times.



*Fig 7. Light I-V curves for various diffusion times highlighting the effect of junction depth (xj) on device performance*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Diffusion Time** | **748 s** | **208 s** | **153 s** | **135 s** | **60 s** |
| Junction Depth (nm) | 1778±411 | 857±163 | 605±158 | 379±145 | 210±136 |
| Voc (V) | 0.54 | 0.56 | 0.57 | 0.58 | 0.56 |
| Jsc (mA/cm2) | 9.33 | 14.98 | 19.32 | 19.85 | 17.22 |
| Fill Factor (%) | 56.90 | 61.98 | 54.50 | 46.81 | 43.02 |
| Rsh (Ω cm2) | 1490 | 1135 | 975 | 178 | 222 |
| Rs (Ω cm2) | 9.61 | 7.71 | 8.42 | 9.55 | 9.95 |
| Efficiency (%) | 3.53 | 5.19 | 6.01 | 5.38 | 4.13 |

*Table 2. Performance parameters for devices with emitter thickness varied by diffusion time*

The thickest emitter (> 1.5 µm) demonstrated excellent shunt resistance (≈ 1500 Ω cm2) but yielded poor values for Jsc of 9.33 mA/cm2 and resultantly the efficiency. This is ascribed to high front surface recombination resulting from the heavily doped emitter. It can be seen that the efficiency increases with decreasing junction depth up to 605 nm. This is largely due to the Jsc which increases with reducing junction depth except for the shortest diffusion time. The open circuit voltage remains essentially constant. The efficiency then drops off for further emitter thickness reductions. This is due to the much poorer fill factors which can be attributed to decreasing shunt resistance and rising series resistance as shown in Table 2.

1. **Conclusions**

The development of Proximity Rapid Thermal Diffusion (PRTD) as a process for fabricating silicon solar cells has been described.

The PRTD process is capable of rapidly diffusing highly doped but shallow emitters using no toxic gases and with total thermal processing times of less than 3 mins.

The diffusion process is significantly improved by the addition of oxygen to the nitrogen carrier gas. The sheet resistance falls from over 300 Ω/□ to ≈ 25 Ω/□ and the uniformity of the diffusion improves by a factor of ten with the addition of 2.5% oxygen to the nitrogen carrier. The addition of oxygen may also be responsible for the attainment of doping concentrations approaching the electronic limit of phosphorus in silicon (3 × 1020 atoms/cm3) at temperatures lower than conventional theory would suggest are possible.

Thick emitters (> 1.5 µm) prepared by the PRTD process demonstrated excellent shunt resistances (≈ 1500 Ω cm2) but yielded poor values for Jsc of 9.33 mA/cm2, believed to be due to high recombination due to the heavily doped emitter. Reduction of the emitter thickness to ≈ 605 nm supported this conclusion as Jsc rose to 19.32 mA/cm2, with only a negligible (≈ 2.5%) fall in fill factor for a total efficiency of 6.01%. Further reduction in emitter thickness to ≈ 379 nm yielded similar values for Jsc but a fall in absolute efficiency (5.38%) due to a falling fill factor. Additional reductions in emitter thickness led to further Jsc (17.22 mA/cm2) and efficiency losses (4.13%), indicating that further process refinement would be necessary to obtain significantly thinner emitters with useful performance.

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**References**

[1] S. Philipps, W. Warmuth, Photovoltaics Report, Freiburg, 2017. https://www.ise.fraunhofer.de/content/dam/ise/de/documents/publications/studies/Photovoltaics-Report.pdf (accessed August 16, 2017).

[2] D. Hernández, T. Trifonov, M. Garín, R. Alcubilla, “Silicon millefeuille”: From a silicon wafer to multiple thin crystalline films in a single step, Appl. Phys. Lett. 102 (2013) 172102. doi:10.1063/1.4803009.

[3] G. Dong, F. Liu, J. Liu, H. Zhang, M. Zhu, Realization of radial p-n junction silicon nanowire solar cell based on low-temperature and shallow phosphorus doping., Nanoscale Res. Lett. 8 (2013) 544. doi:10.1186/1556-276X-8-544.

[4] H. Kim, J. Kim, E. Lee, D.-W. Kim, J.-H. Yun, J. Yi, Effect of the short collection length in silicon microscale wire solar cells, Appl. Phys. Lett. 102 (2013) 193904. doi:10.1063/1.4804581.

[5] F. Milési, M. Coig, J.-F. Lerat, T. Desrues, J. Le Perchec, A. Lanterne, L. Lachal, F. Mazen, Homojunction silicon solar cells doping by ion implantation, Nucl. Instruments Methods Phys. Res. Sect. B Beam Interact. with Mater. Atoms. In Press (2017). doi:10.1016/j.nimb.2017.06.020.

[6] D. Mathiot, a. Lachiq, a. Slaoui, S. Noël, J.C. Muller, C. Dubois, Phosphorus diffusion from a spin-on doped glass (SOD) source during rapid thermal annealing, Mater. Sci. Semicond. Process. 1 (1998) 231–236. doi:10.1016/S1369-8001(98)00045-6.

[7] B. Terheiden, CVD Boron Containing Glasses – An Attractive Alternative Diffusion Source for High Quality Emitters and Simplified Processing - A Review, Energy Procedia. 92 (2016) 486–492. doi:10.1016/j.egypro.2016.07.131.

[8] X. Wang, K.L. Pey, C.H. Yip, E.A. Fitzgerald, D.A. Antoniadis, Vertically arrayed Si nanowire/nanorod-based core-shell p-n junction solar cells, J. Appl. Phys. 108 (2010) 124303. doi:10.1063/1.3520217.

[9] W. Zagozdzon-Wosik, P.B. Grabiec, G. Lux, Silicon doping from phosphorus spin-on dopant sources in proximity rapid thermal diffusion, J. Appl. Phys. 75 (1994) 337–344. doi:10.1063/1.355855.

[10] R. Keding, D. Stuwe, M. Kamp, C. Reichel, A. Wolf, R. Woehl, D. Borchert, H. Reinecke, D. Biro, Co-Diffused Back-Contact Back-Junction Silicon Solar Cells without Gap Regions, IEEE J. Photovoltaics. 3 (2013) 1236–1242. doi:10.1109/JPHOTOV.2013.2274382.

[11] A. Oates, F.J. Cabrera-España, A. Agrawal, H.S. Reehal, Fabrication and characterisation of Si micropillar PV structures, Mater. Res. Innov. 18 (2014) 500–504. doi:10.1179/1433075X14Y.0000000244.

[12] M. Nolan, T. Perova, R.A. Moore, H.S. Gamble, Boron diffusion from a spin-on source during rapid thermal processing, J. Non. Cryst. Solids. 254 (1999) 89–93. doi:10.1016/S0022-3093(99)00379-8.

[13] R. Elbersen, R.M. Tiggelaar, A. Milbrat, G. Mul, H. Gardeniers, J. Huskens, Controlled doping methods for radial p/n junctions in silicon, Adv. Energy Mater. 5 (2015) 1–8. doi:10.1002/aenm.201401745.

[14] R.S. Muller, T.I. Kamins, M. Chan, Device electronics for integrated circuits, 3rd ed., John Wiley & Sons, New York, 2003.

[15] S.K. Ghandhi, Diffusion Systems for Silicon, in: VLSI Fabr. Princ. Silicon Gall. Arsenide, 2nd ed., Wiley, New York, 1994: pp. 209–216.

[16] U. Gösele, H. Strunk, High-temperature diffusion of phosphorus and boron in silicon via vacancies or via self-interstitials?, Appl. Phys. 20 (1979) 265–273. doi:10.1007/BF00894994.

[17] A. Kazor, Space-charge oxidant diffusion model for rapid thermal oxidation of silicon, J. Appl. Phys. 77 (1995) 1477. doi:10.1063/1.358896.

[18] K. Taniguchi, K. Kurosawa, M. Kashiwagi, Oxidation Enhanced Diffusion of Boron and Phosphorus in (100) Silicon, J. Electrochem. Soc. 127 (1980) 2243. doi:10.1149/1.2129384.

[19] P.B. Grabiec, W. Zagozdzon-Wosik, G. Lux, Kinetics of phosphorus proximity rapid thermal diffusion using spin-on dopant source for shallow junctions fabrication, J. Appl. Phys. 78 (1995) 204–211. doi:10.1063/1.360653.

[20] S.K. Ghandhi, Impurity Behaviour: Silicon, in: VLSI Fabr. Princ. Silicon Gall. Arsenide, 2nd ed., Wiley, New York, 1994: pp. 183–196.